



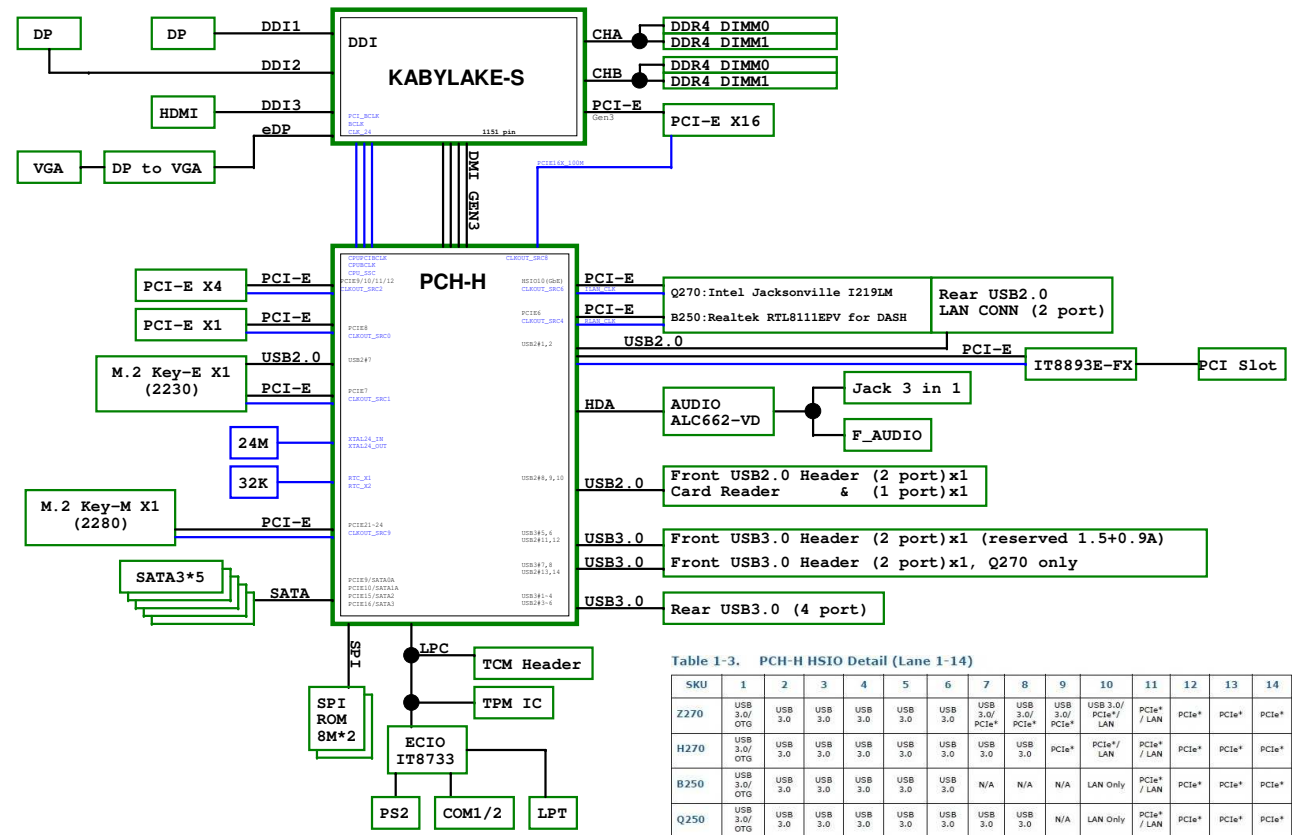
Q27H4-AM

Rev:1.0

ECS
CONFIDENTIAL

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PCH-H SKUs

Features	Z270	H270	B250	Q250	Q270
Intel® Rapid Storage Technology	Full Features ¹	Full Features ¹	AHCI Mode	AHCI Mode	Full Features ¹
Total USB 3.0 Ports	Up to 10	8	6	8	Up to 10
Total USB 2.0 Ports	14 ³	14 ³	12 ²	14 ³	14 ³
Total SATA 6 Gb/s (Gen3) Ports	Up to 6	Up to 6	Up to 6	Up to 6	Up to 6
Total PCI Express* 3.0 Lanes	Up to 24	Up to 20	Up to 12	Up to 14	Up to 24
Total Controllers for Intel® RST for PCIe* Storage Devices	3 ⁵	2 ⁴	1	1	3 ⁵
Processor PCI Express* 3.0 Lanes Configuration Support	1x16 or 2x8 or 1x8+2x4	1x16	1x16	1x16	1x16 or 2x8 or 1x8+2x4
Processor Over clocking	No	No	No	No	Yes

Notes:

1. Full featured includes SATA RAID 0/1/5/10 support
2. USB 2.0 port numbers: 1-12
3. USB 2.0 port numbers: 1-14
4. Intel® RST PCIe* supports RAID configuration 0/1.
5. Intel® RST PCIe* supports RAID configuration 0/1/5

HSIO Multiplexing on KBL PCH-H

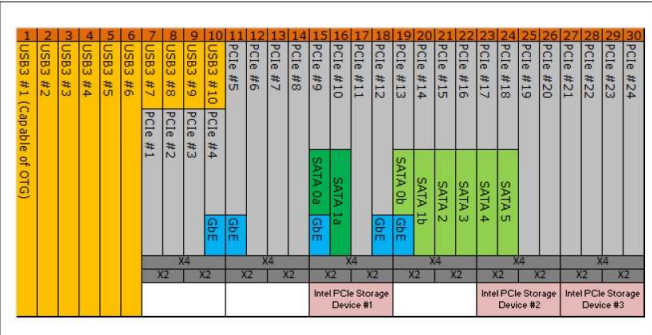


Table 1-3. PCH-H HSIO Detail (Lane 1-14)

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Z270	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*/LAN	PCIe*/LAN	PCIe*	PCIe*	PCIe*
H270	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	PCIe*	PCIe*/LAN	PCIe*/LAN	PCIe*	PCIe*	PCIe*
B250	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	LAN Only	PCIe*/LAN	PCIe*	PCIe*	PCIe*
Q250	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	LAN Only	PCIe*/LAN	PCIe*	PCIe*	PCIe*
Q270	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*/LAN	PCIe*/LAN	PCIe*	PCIe*	PCIe*

Table 1-4. PCH-H HSIO Detail (Lane 15-26) (Sheet 1 of 2)

SKU	15 ¹	16 ¹	17	18	19 ¹	20 ¹	21	22	23	24	25	26
Z270 (See Note 2)	PCIe*/LAN / SATA0a	PCIe*/SATA1a	PCIe*	PCIe*/LAN	PCIe*/LAN / SATA0b	PCIe*/SATA1b	PCIe*/SATA2	PCIe*/SATA3	PCIe*/SATA4	PCIe*/SATA5	PCIe*	PCIe*
H270 (See Note 2)	PCIe*/LAN / SATA0a	PCIe*/SATA1a	PCIe*	PCIe*/LAN	PCIe*/LAN / SATA0b	PCIe*/SATA1b	PCIe*/SATA2	PCIe*/SATA3	SATA4	SATA5	PCIe*	PCIe*
B250	PCIe*/LAN / SATA0a	PCIe*/SATA1a	PCIe*	PCIe*/LAN	SATA0b	SATA1b	SATA2	SATA3	SATA4	SATA5	N/A	N/A
Q250	PCIe*/LAN / SATA0a	PCIe*/SATA1a	PCIe*	PCIe*/LAN	PCIe*/LAN / SATA0b	PCIe*/SATA1b	SATA2	SATA3	SATA4	SATA5	N/A	N/A
Q270 (See Note 2)	PCIe*/LAN / SATA0a	PCIe*/SATA1a	PCIe*	PCIe*/LAN	PCIe*/LAN / SATA0b	PCIe*/SATA1b	PCIe*/SATA2	PCIe*/SATA3	PCIe*/SATA4	PCIe*/SATA5	PCIe*	PCIe*

Notes:

1. Refer to Flexible I/O chapter for the additional information.
2. Only the highlighted (in bold text) PCIe* lanes are capable of supporting the Intel® RST for PCIe* Storage (remapping), configured as x2 or x4.

Table 1-5. PCH-H HSIO Detail (Lane 27-30)

SKU	27	28	29	30
Z270 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*
H270 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*
B25 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*
Q250 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*
Q270 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*

Note: All PCIe* lanes on HSIO 27 - 30 are capable of supporting the Intel® RST for PCIe* Storage Device, configured as x2 or x4.

PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPP_D7	3VSB	GPP_D7_CASEOPEN (reserved)	GPIO(GPI)
GPP_D6	3VSB	GPP_D6_BIOSWP	GPIO(GPI)
GPP_D5	3VSB	GPP_D5_BIOS_WP	GPIO(GPI)
GPD10	ATX_3VSB	GPD10 (ME disable by SW)	SLP_S5#
GPD2	ATX_3VSB	ILAN_WAKE_L	LAN_WAKE#
GPD0	ATX_3VSB	RLAN_PWR_EN (only for for B25 sku)	BATLOW#
GPD11	ATX_3VSB	LAN_DIS_L	LANPHYPC
GPP_A12	3VSB	GPP_A12_TPM H:with on-board TPM L:W/O on-board TPM	GPIO(GPI)
GPP_G16	3VSB	LPC_PME_L	GPIO(GPI)
GPP_G13	VCC3	HDPANEL_DETECT (reserved)	GPIO(GPI)
GPP_A14	VCC3	LPCPD_L	SUS_STAT#
GPP_A0	VCC3	KBRST_L_RC	RCIN#
GPP_A6	VCC3	SERIRQ	SERIRQ
GPP_A5	N/A	LPC_FRAME_L	LFRAME#
GPP_A1	N/A	LPC_LAD0	LAD0
GPP_A2	N/A	LPC_LAD1	LAD1
GPP_A3	N/A	LPC_LAD2	LAD2
GPP_A4	N/A	LPC_LAD3	LAD3
GPP_A9	N/A	PCH_SIO_24M	CLKOUT_LPC0
GPP_A10	N/A	TCM_TPM_24M	CLKOUT_LPC1
GPP_B3	VCC3	BT_DISABLE_L L:disable	GPIO(GPI)
GPP_B17	VCC3	WLAN_DISABLE_L L:disable	GPIO(GPI)
GPP_E8	VCC3	SATALED_L	SATA_LED#
GPP_F16	3VSB	GPP_F16 H: USB power enable	GPIO(GPI)
GPP_I0	N/A	DDPB_HPD0	DDPB_HPD0
GPP_I1	N/A	DDPC_HPD1	DDPC_HPD1
GPP_I2	N/A	DDPD_HPD2	DDPD_HPD2
GPP_I2	N/A	DDPE_HPD3	DDPE_HPD3
GPP_G23	3VSB	GPP_G22 H:default BIOS L:on-board VGA	GPIO(GPI)
GPP_F22	VCC3	GPP_F22_PCIEIRST (PCIEx16 SW RST#)	GPIO(GPI)
GPD9	ATX_3VSB	PCH_RI_L L:RI# wake up	SLP_WLAN#
GPP_H0	3VSB	ILAN_CLKREQ	SRCLKREQ0#
GPP_B6	3VSB	M2CLK_REQ1_L	SRCLKREQ1#
GPP_E0	3VSB	GPP_E0_OBR (ACER's OBR)	GPIO(GPI)
GPP_H14	3VSB	GPP_H14 (ACER reserved GPIO)	GPIO(GPI)
GPP_H15	3VSB	GPP_H15 (ACER reserved GPIO)	GPIO(GPI)
GPP_A11	3VSB	PME_L	PME#
GPP_B7	3VSB	PEX4X_REQ2_L	SRCLKREQ2#
GPP_D0	DIMM_5VDUAL	SIO_LED0	GPIO(GPI)
GPP_D1	DIMM_5VDUAL	SIO_LED1	GPIO(GPI)

ECIO-GPIO function

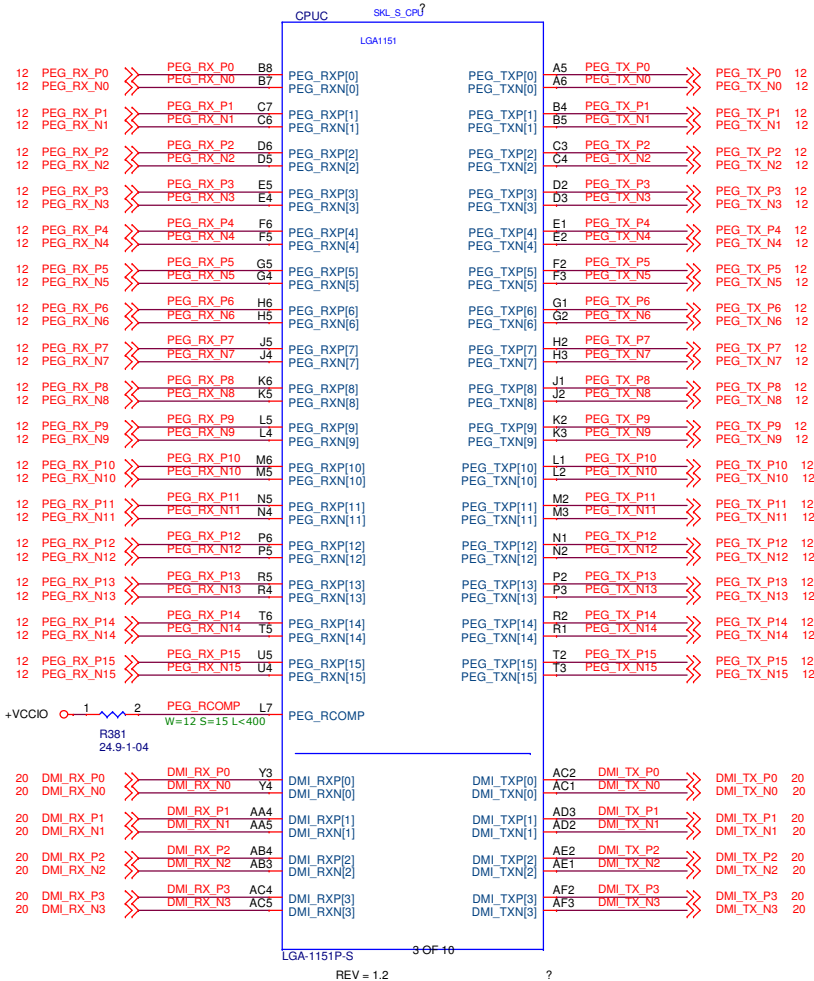
Pin Name	Power Well	Usage	Default Status
GP33	3VSB	Wake up by Monitor(DP1)	SUSACK(DOD8)
GP34	3VSB	Wake up by Monitor(DP2)	SUWARN#(DI)
GP35	3VSB	Wake up by Monitor(VGA)	FAN_TAC4(DI)
GP36	3VSB	Wake up by Monitor(HDMI)	FAN_CTL3(DOD8)
GP37	ATX_5VSB	DP Wake up by Monitor control	FAN_TAC3(DI)
RI2#/ GP17	3VSB	VGA/HDMI Wake up by Monitor control	RI2#(DI)
GP16	3VSB	basic health function	5VSB_CTRL#(DOD8)
GP31	3VSB	sleep mode wake up	PWNOUT(DOD8)
GP41	3VSB	GPP_E7_THERM	PWROK2(DOD8)

PCH_CPU-Strap

Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU F10 lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5:6	CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express	PCIEL6X
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP enable:	0 = Enable
CFG7	CFG[7]: PEG Training:	1 = (default) PEG Train Immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lanes.	
SPKR/GPP_B14	Top Swap Override	0 =Disable "Top Swap" mode. (Default)
GSPI0_MOSI/GPP_B18	No Reboot	0 =Disable "No Reboot" mode
SMBALERT#/GPP_C2	TLS Confidentiality	1 =EnableIntel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel BMA (Small Business Advantage) with TLS
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit BBS	0=SPI
SML0ALERT#/GPP_C5	eSPI or LPC	0 =LPCIs selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 =Enable security measures defined in the Flash Descriptor. 1 =Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPB_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.

Interrupt mapping

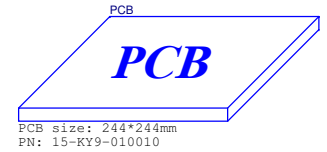
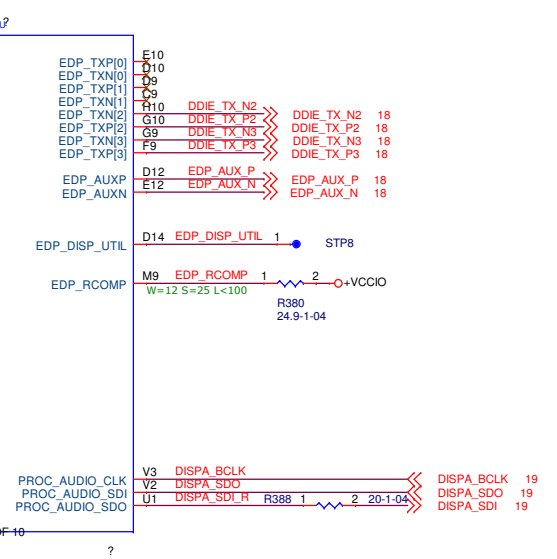
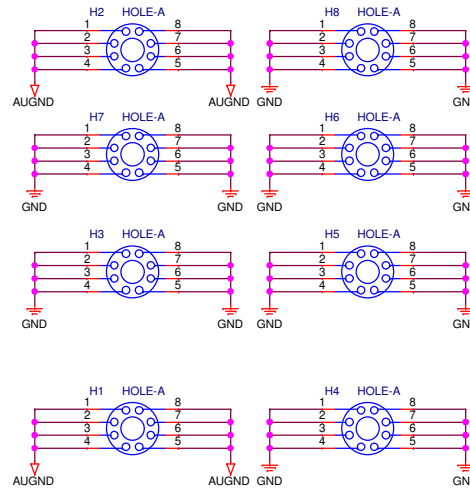
Function	INT#port	PCIe*1 port	Device
ILAN	INTB#	Port4	WG1219LM
RLAN	INTB#	Port6	RTL8111EPV
SATA	INTA#	NA	SATA3.0

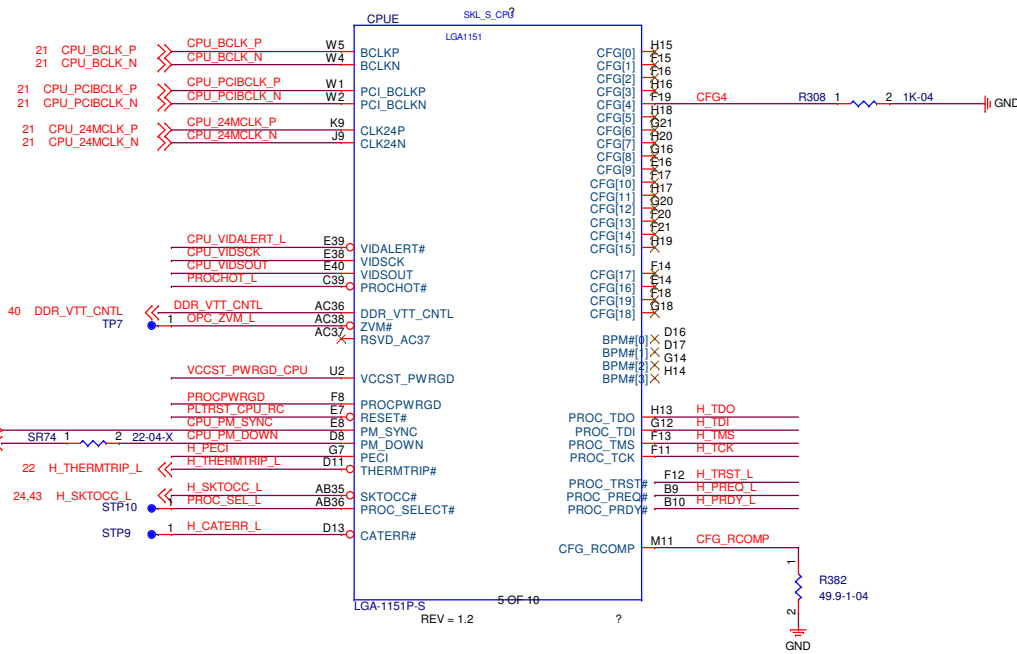


DP1

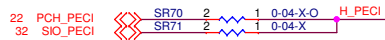
DP2

HDMI





PECI



Asynchronous & Sideband Signal

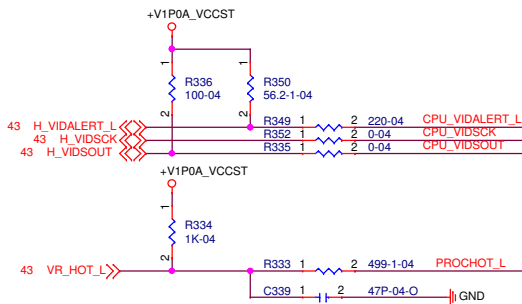


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

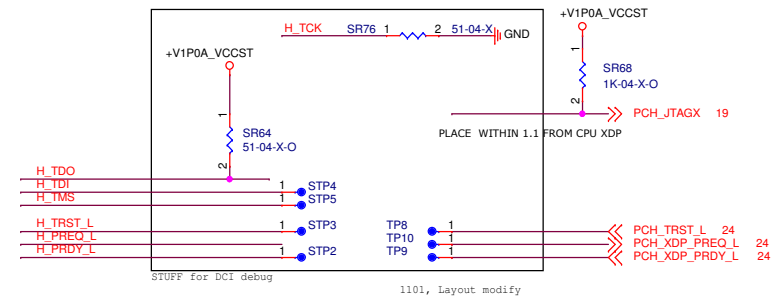
			Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

- Notes:**
- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
 - In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.
- For example:
- When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

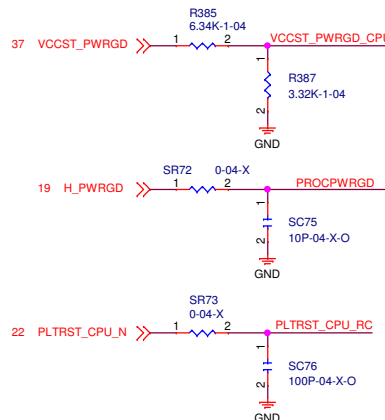
CFG[0:15] Configuration note

- CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
 - 1 = (Default) Normal Operation; No stall.
 - 0 = Stall.
- CFG[1]:** Reserved configuration lane.
- CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
 - 1 = Normal operation
 - 0 = Lane numbers reversed.
- CFG[3]:** Reserved configuration lane.
- CFG[4]:** eDP enable:
 - 1 = Disabled.
 - 0 = Enabled.
- CFG[5:6]:** PCI Express* Bifurcation
 - 00 = 1 x8, 2 x4 PCI Express*
 - 01 = reserved
 - 10 = 2 x8 PCI Express*
 - 11 = 1 x16 PCI Express*
- CFG[7]:** PEG Training:
 - 1 = (default) PEG Train immediately following RESET# de assertion.
 - 0 = PEG Wait for BIOS for training.
- CFG[19:8]:** Reserved configuration lanes.

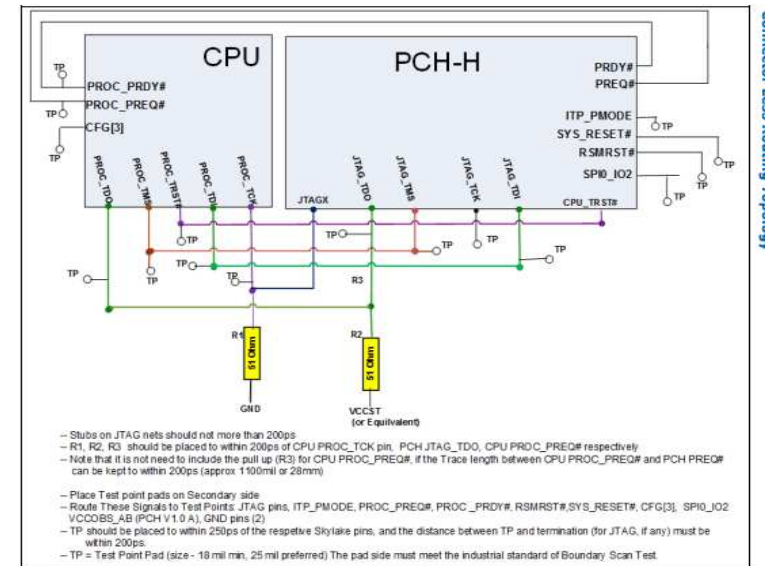
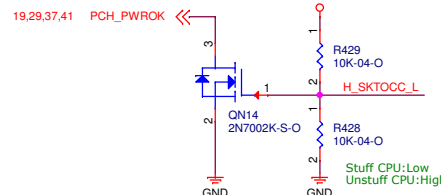
H_PREQ_L SR77 1 2 51-04-X-O V1P0A_VCCST
UNSTUFF for merged X-O
PLACE NEAR CPU WITHIN 1.1 INCH



Processor Power Good



SKTOCC#

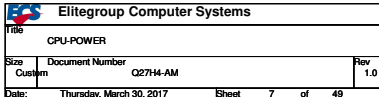


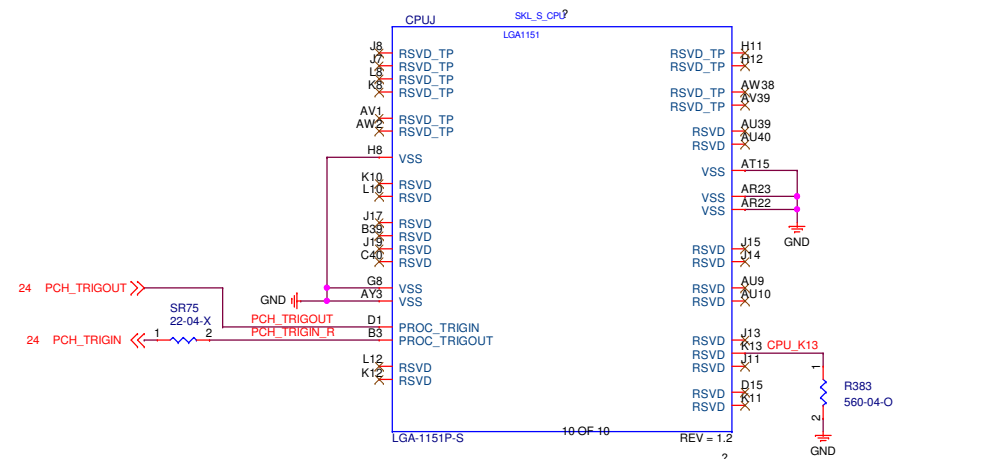
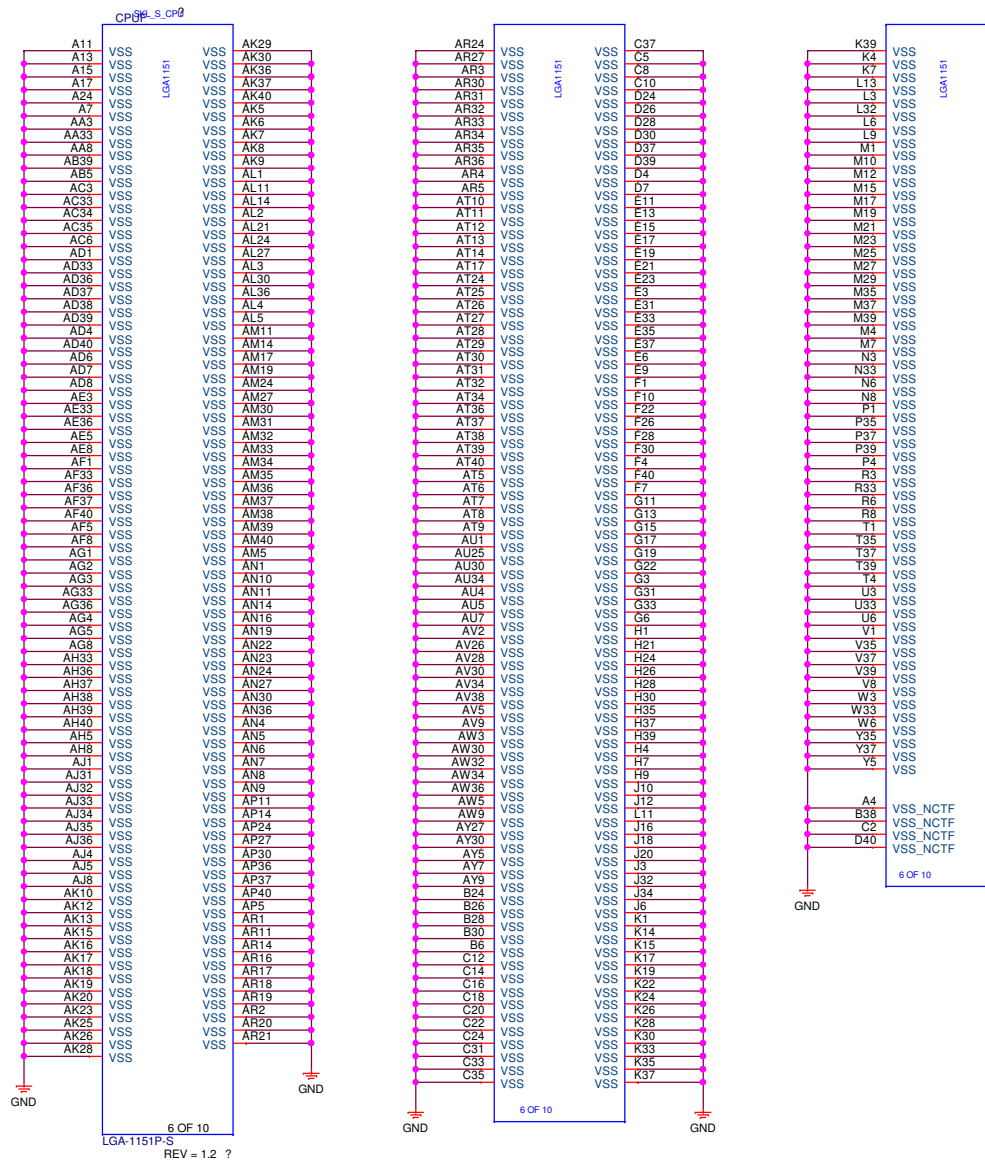
- Stubs on JTAG nets should not more than 200ps
- R1, R2, R3 should be placed to within 200ps of CPU PROC_TCK pin, PCH JTAG_TDO, CPU PROC_PREQ# respectively
- Note that it is not need to include the pull up (R3) for CPU PROC_PREQ#, if the Trace length between CPU PROC_PREQ# and PCH PREQ# can be kept to within 200ps (approx. 150mm or 28mm)
- Place Test point pads on Secondary side
- Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#, SYS_RESET#, CFG[3], SPI0_IO2, VCC0B5_A0 (PCH V1.0 A), GND pins (2)
- TP should be placed to within 250ps of the respective Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
- TP = Test Point Pad (size - 18 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.

9	M_DATA_A[0..63]	《	M_DATA_A[0..63]
9	M_CLK_A_P[0..3]	《	M_CLK_A_P[0..3]
9	M_CLK_A_N[0..3]	《	M_CLK_A_N[0..3]
9	M_CKE_A[0..3]	《	M_CKE_A[0..3]
9	M_CS_A_L[0..3]	《	M_CS_A_L[0..3]
9	M_ODT_A[0..3]	《	M_ODT_A[0..3]
9	M_MA_A[0..15]	《	M_MA_A[0..15]
9	M_DQS_A_P[0..7]	《	M_DQS_A_P[0..7]
9	M_DQS_A_N[0..7]	《	M_DQS_A_N[0..7]

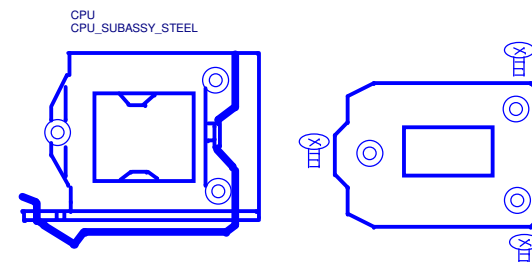
10	M_DATA_B[0..63]	10	M_DATA_B[0..63]
10	M_CLK_B_P[0..3]	10	M_CLK_B_P[0..3]
10	M_CLK_B_N[0..3]	10	M_CLK_B_N[0..3]
10	M_CKE_B[0..3]	10	M_CKE_B[0..3]
10	M_CS_B_L[0..3]	10	M_CS_B_L[0..3]
10	M_ODT_B[0..3]	10	M_ODT_B[0..3]
10	M_MA_B[0..15]	10	M_MA_B[0..15]
10	M_DQS_B_P[0..7]	10	M_DQS_B_P[0..7]
10	M_DQS_B_N[0..7]	10	M_DQS_B_N[0..7]



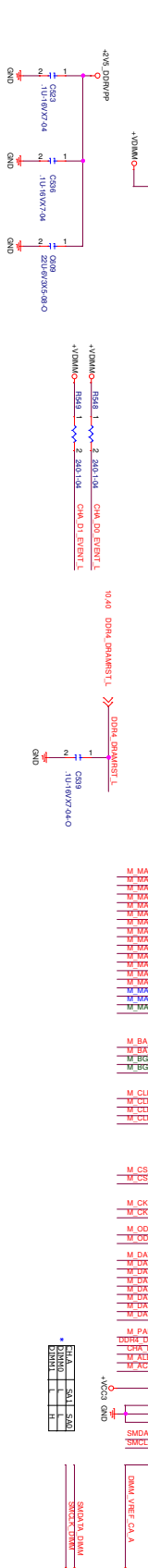
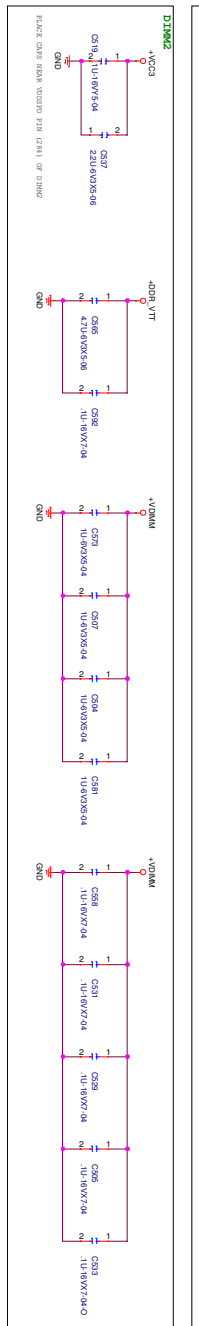
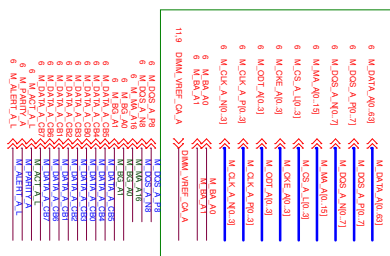


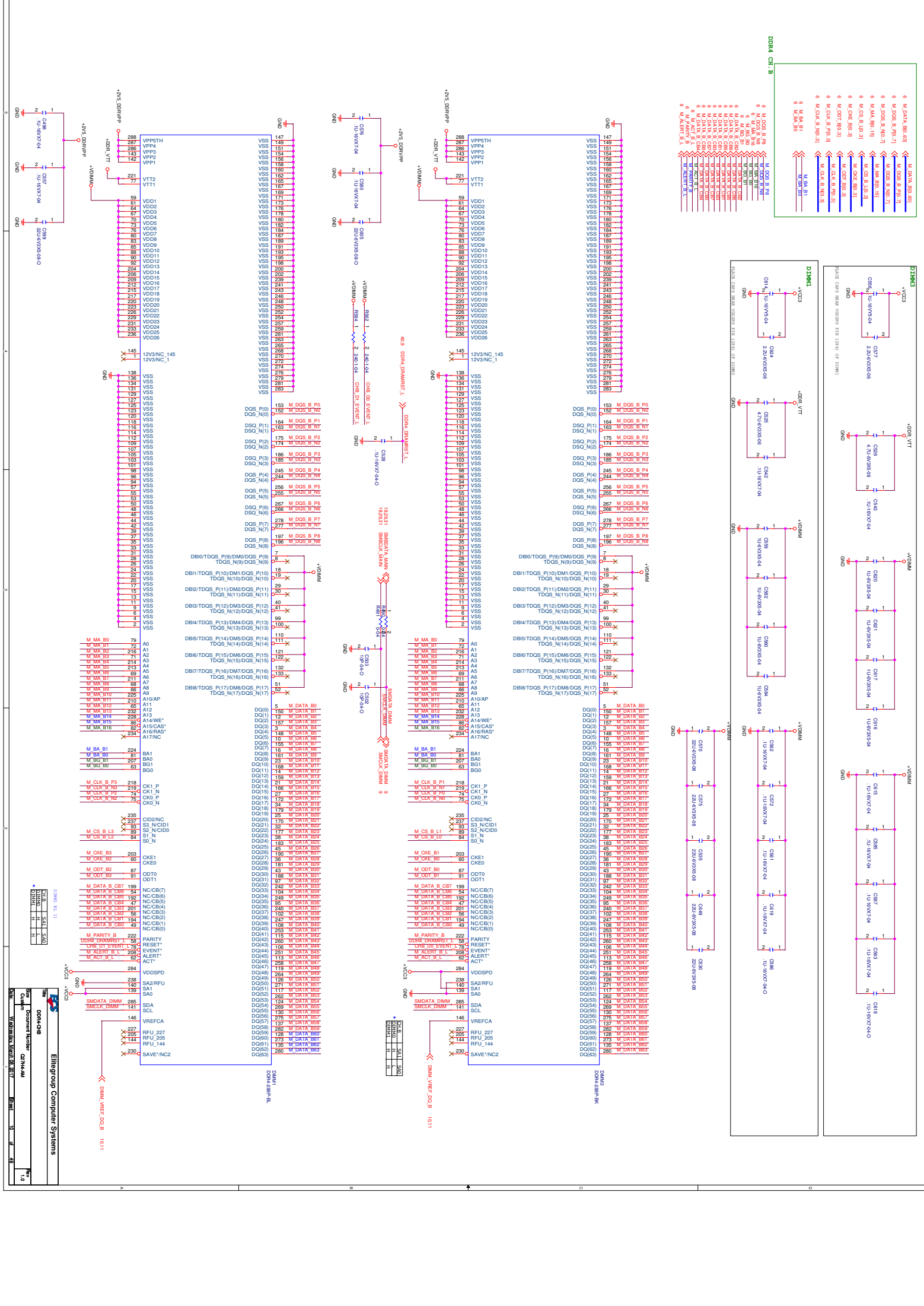


CPU Socket (SMD phase)
P/N:11-018-115133
SOCKET.CPU..LGA 1151P SMD..G/F...BLACK.AZIF0049-P002C...HF.LEAD-FREE.LOTES

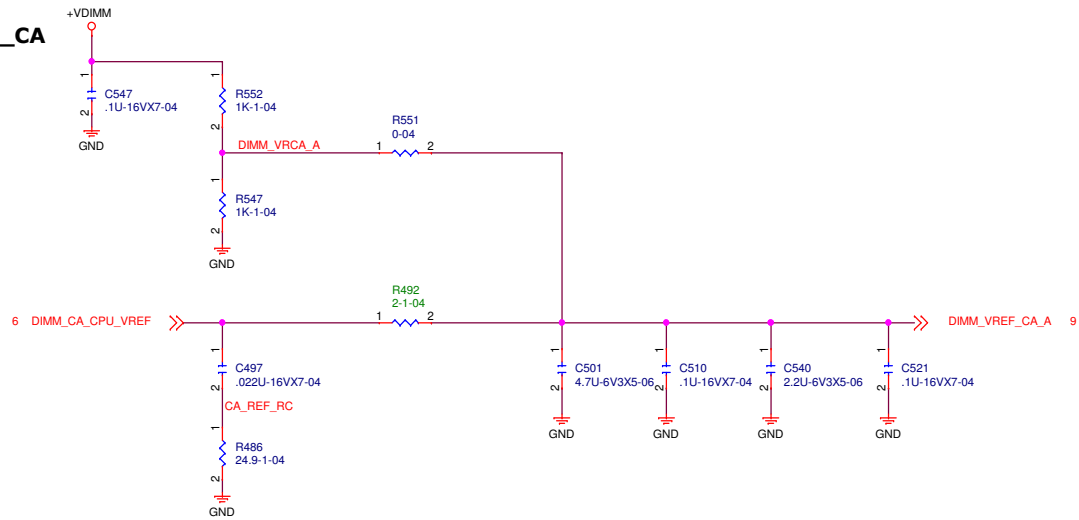


CPU Steel (T/U pahse)
P/N:20-800-005911 SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....
ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES

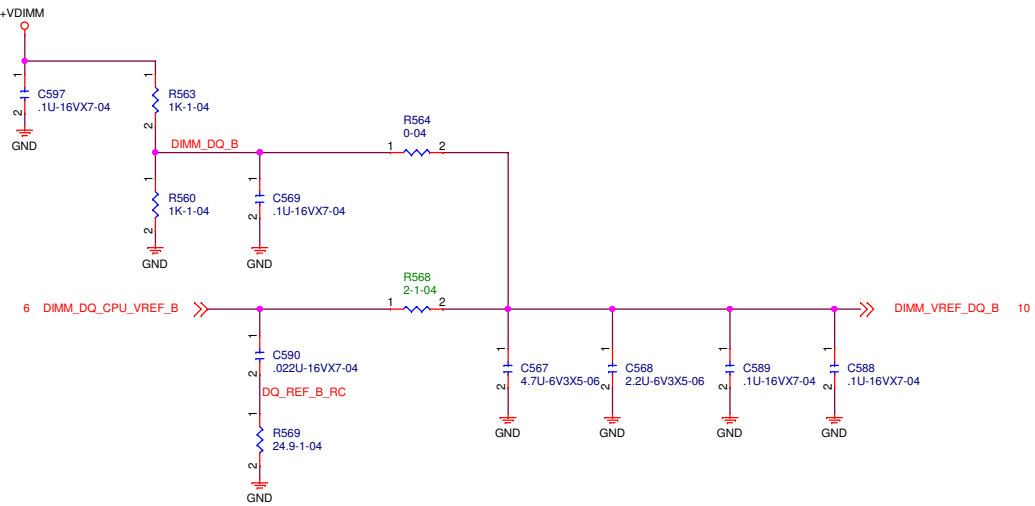


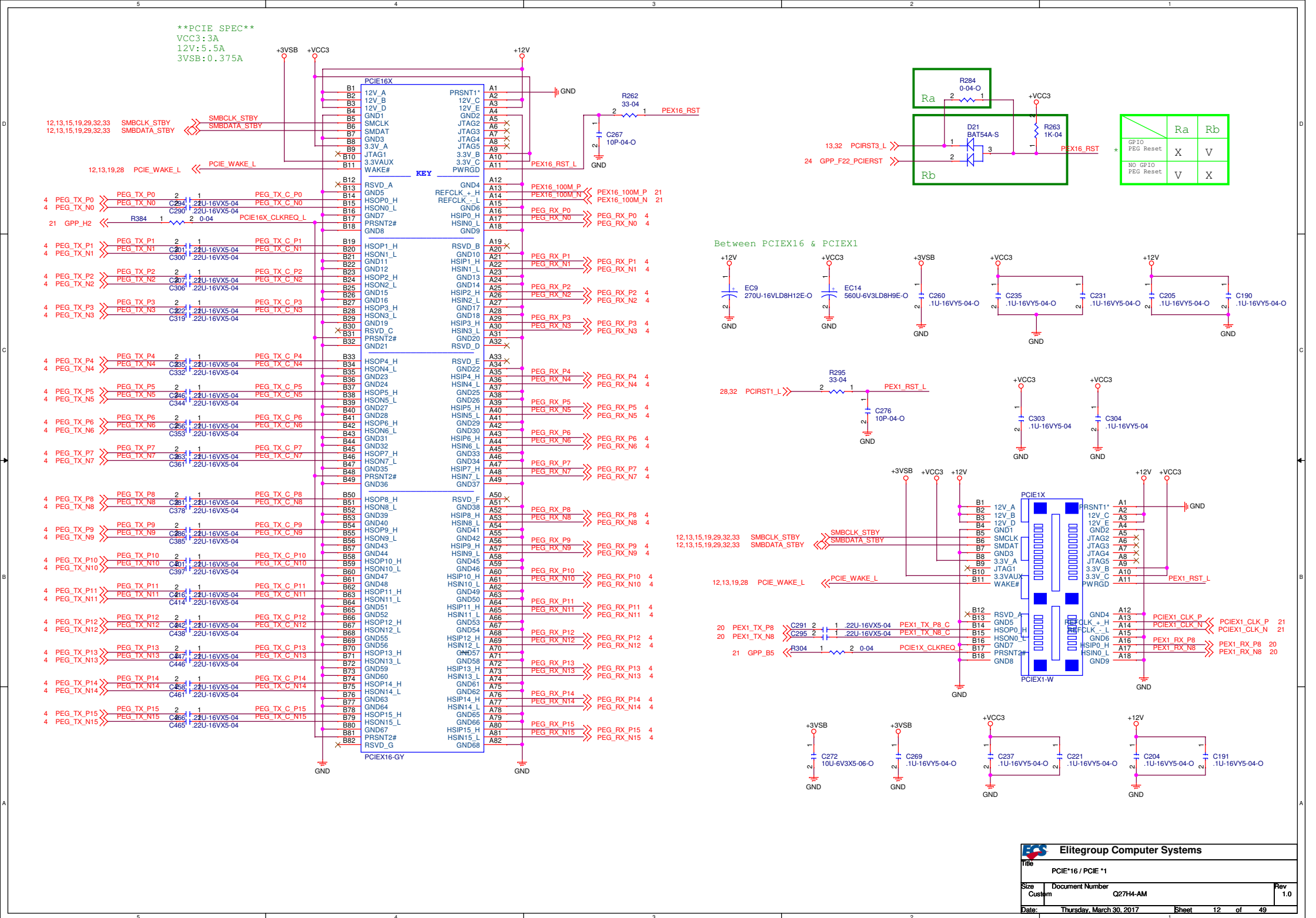


DIMM_VREF_CA



DIMM_VREF_DQ





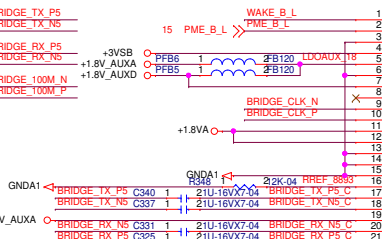
15 AD[31..0] <<> AD[31..0]
 15 C_BE_L[3..0] <<> C_BE_L[3..0]
 15 PM66EN <<> PM66EN
 15 FRAME_L <<> FRAME_L
 15 IRDY_L <<> IRDY_L
 15 TRDY_L <<> TRDY_L
 15 STOP_L <<> STOP_L
 15 DEVSEL_L <<> DEVSEL_L
 15 PAR <<> PAR
 15 SERR_L <<> SERR_L
 15 PERR_L <<> PERR_L
 15 LOCK_L <<> LOCK_L
 15 PCICLK0 <<> PCICLK0
 15 INTA_L <<> INTA_L
 15 INTB_L <<> INTB_L
 15 INTC_L <<> INTC_L
 15 INTD_L <<> INTD_L
 15 REQ0_L <<> REQ0_L
 15 REQ1_L <<> REQ1_L
 15 GNT0_L <<> GNT0_L
 15 PCIRST_L <<> PCIRST_L

20,32,33 PCH_PLTRST_L <<> PCH_PLTRST_L

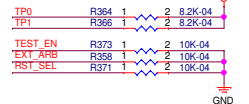
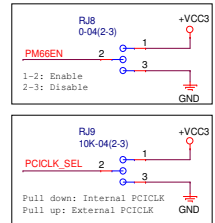
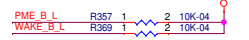
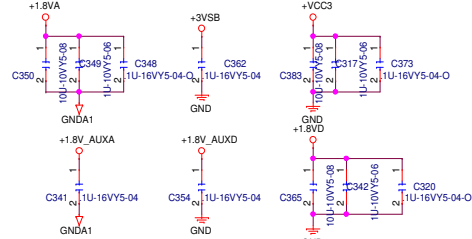
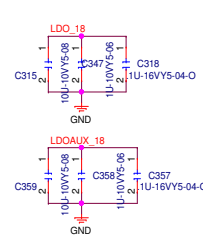
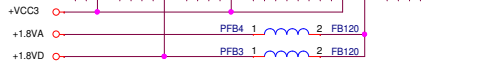
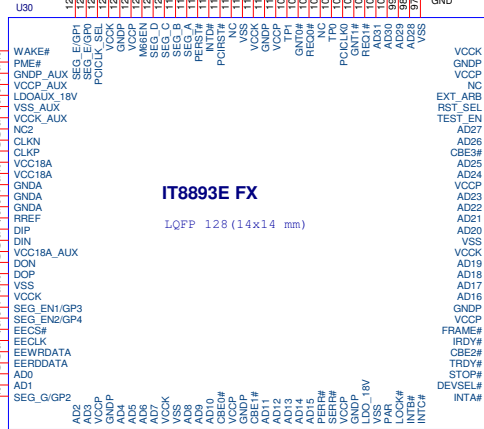
PCH=>

20 BRIDGE_TX_P5 <<> BRIDGE_TX_P5
 20 BRIDGE_TX_N5 <<> BRIDGE_TX_N5
 20 BRIDGE_RX_P5 <<> BRIDGE_RX_P5
 20 BRIDGE_RX_N5 <<> BRIDGE_RX_N5
 21 BRIDGE_100M_N <<> BRIDGE_100M_N
 21 BRIDGE_100M_P <<> BRIDGE_100M_P

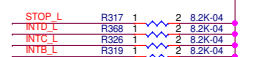
BRIDGE_100M_N 1 2 BRIDGE_CLK_N
 BRIDGE_100M_P 1 2 BRIDGE_CLK_P



IT8893E FX
 LQFP 128 (14x14 mm)



PCI BUS 5V external pull up 2.7Kohm
 PCI BUS 3.3V external pull up 8.2Kohm

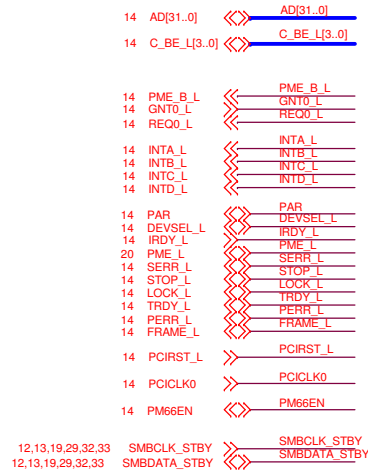


PCIE CLK PCB layout note:
 To meet Differential Impedance :100 ohm +/- 15%
 To meet Single-ended Impedance :50 ohm +/- 15%
 CLKP and CLKN trace width:7 mils
 Space between CLKP and CLKN:14 mils
 L1 & L2 height:5 mils
 The signal traces Number of vias: 4 (Max.)
 The signal trace above analog GND plane
 Spacing from other groups:>25 mils
 Total trace length: 12 inches (Max.)
 The size of R4;R5 is "0402"

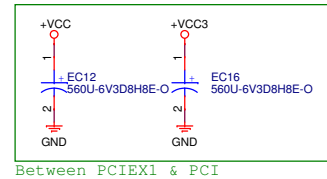
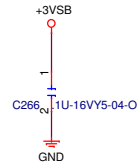
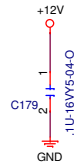
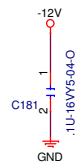
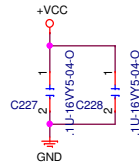
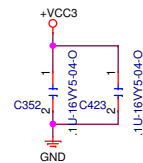
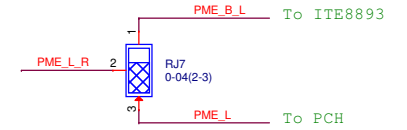
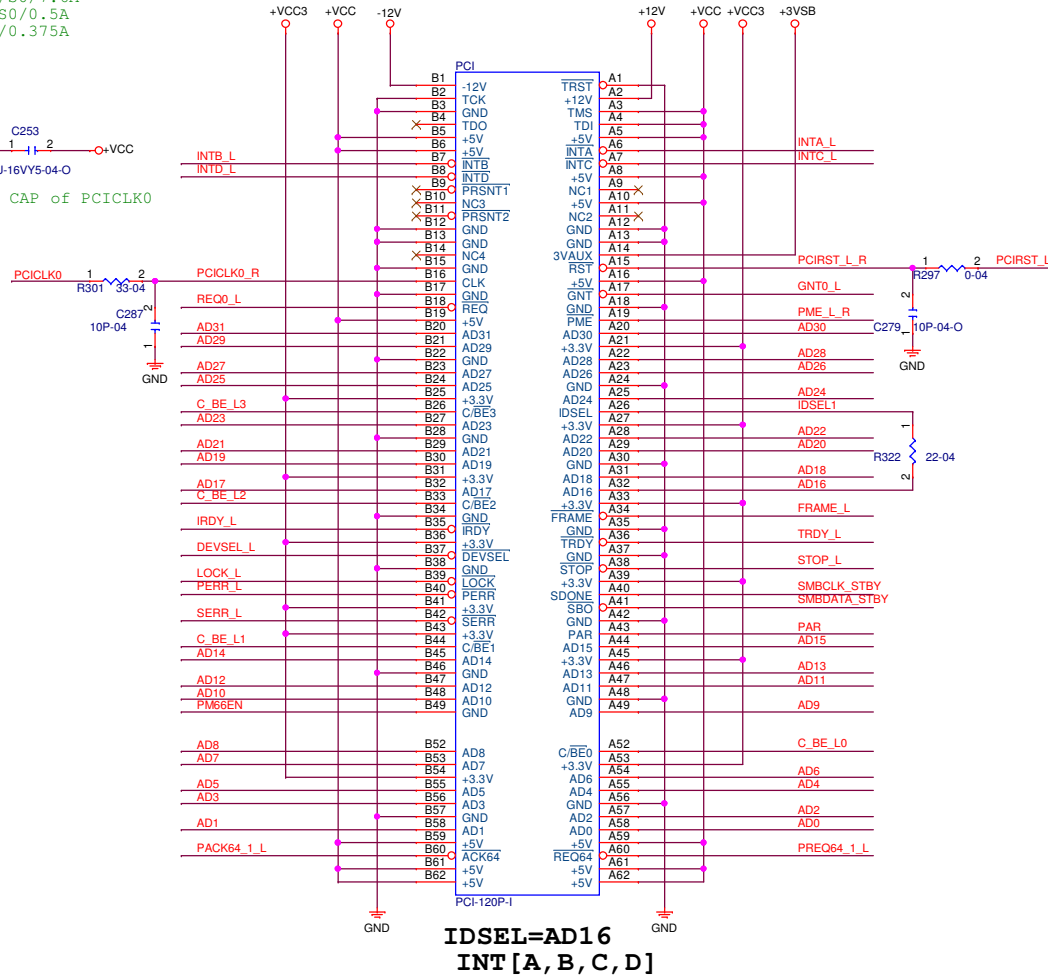
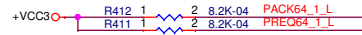
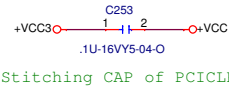
The size of R6;R7 is "0402"

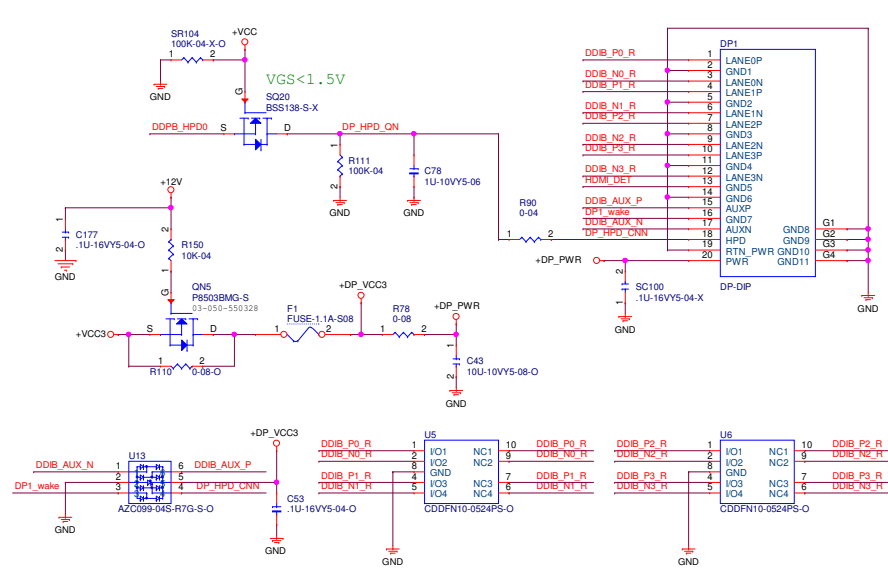
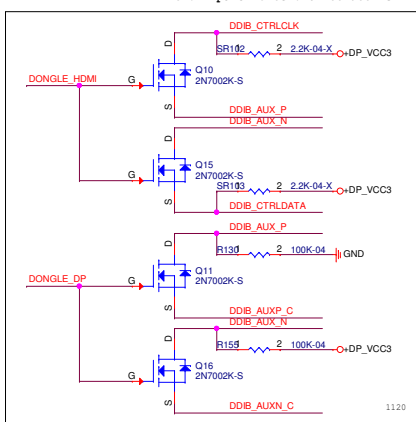
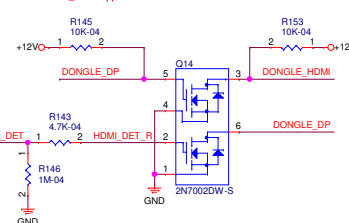
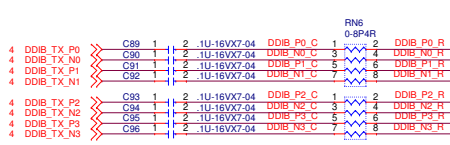
PCIE DIP;DIN;DOP;DON PCB layout note:
 To meet Differential Impedance :85 ohm +/- 15%
 To meet Single-ended Impedance :50 ohm +/- 15%
 PCIE DIP and DIN trace width:9.5 mils
 PCIE DOP and DON trace width:9.5 mils
 Space between DIP/DIN and DOP/DON:14.5 mils
 L1 & L2 height:5 mils
 The signal traces Number of vias: 2 (Max.)
 The signal trace above analog GND plane
 Spacing from other groups:>25 mils
 Total trace length: 12 inches (Max.)

The size of C24;C25 is "0402"



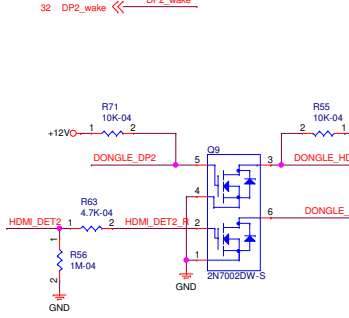
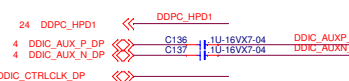
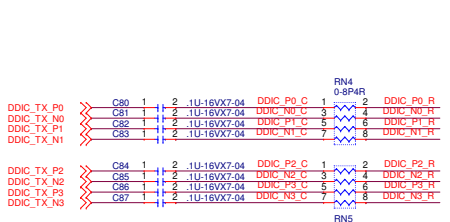
PCI Slot
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A



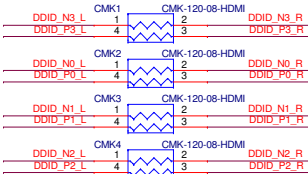
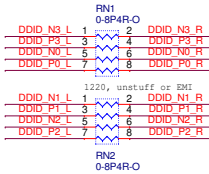
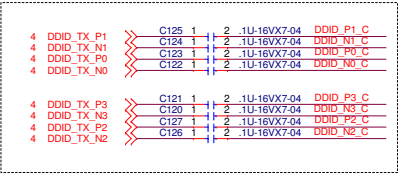


DP1

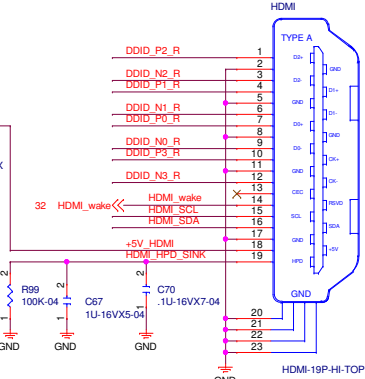
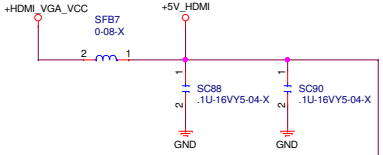
DP2



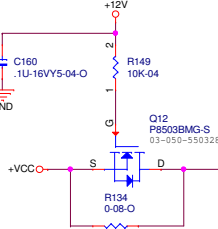
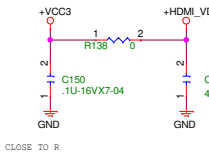
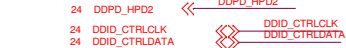
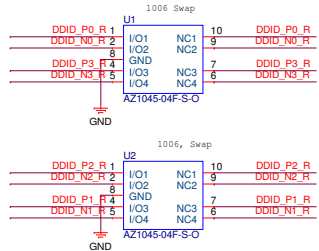
HDMI



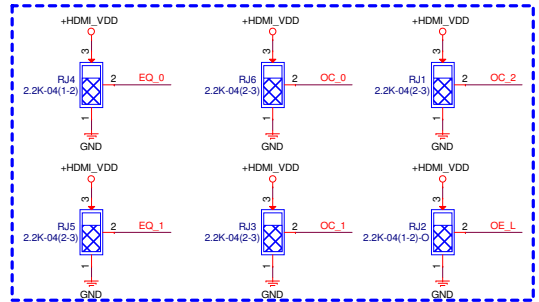
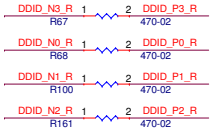
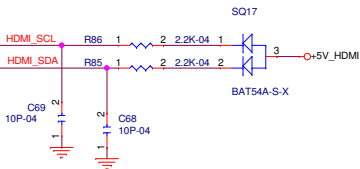
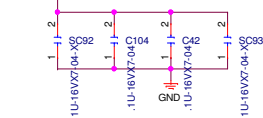
CHOKE part number:
16-400-121143



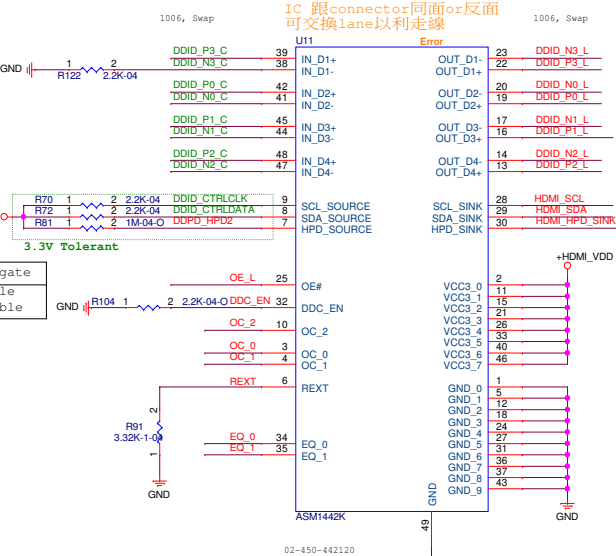
HDMI Connector Pin13:CEC
沒有使用必須空接(Floating)
避免HDCP 測試 FAIL



+HDMI_VDD CLOSE TO U39 VDD PIN, 兩PIN一個
(< 70 mil) and use 10 mil trace width.



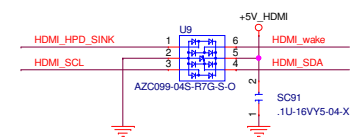
RQ1=1, RQ0=0 for 4K2K. 201702232, CG0=1,CG1=1,CG2=1 for SI

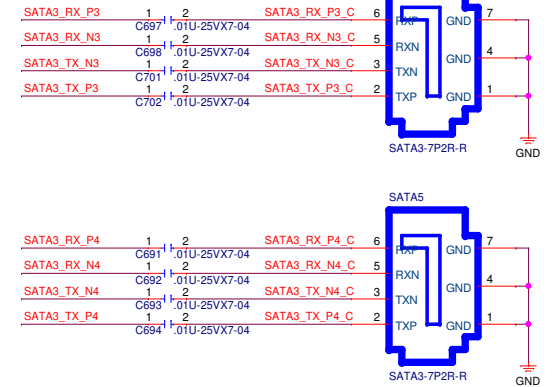
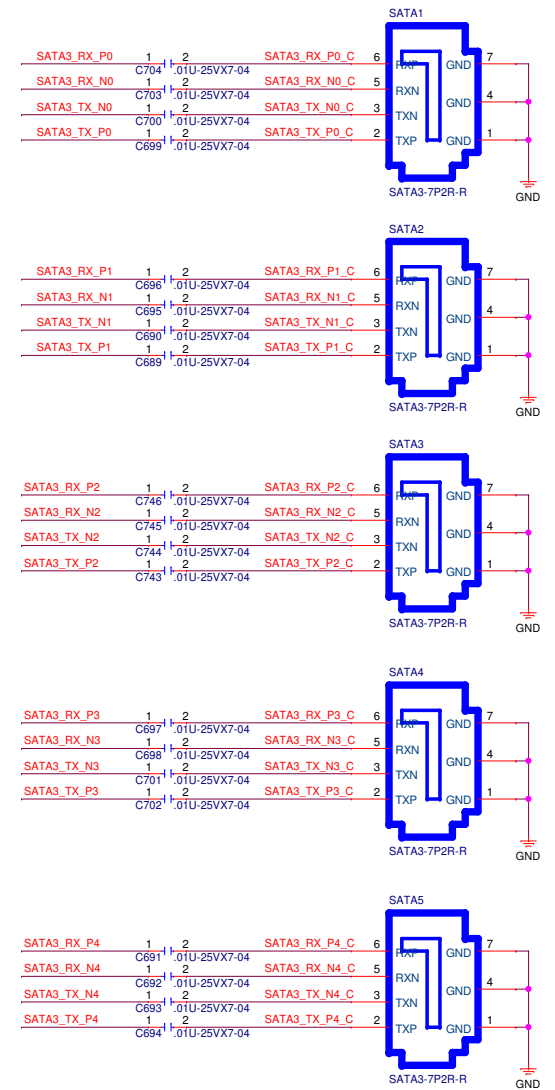


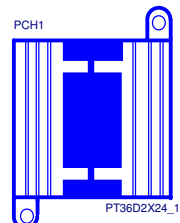
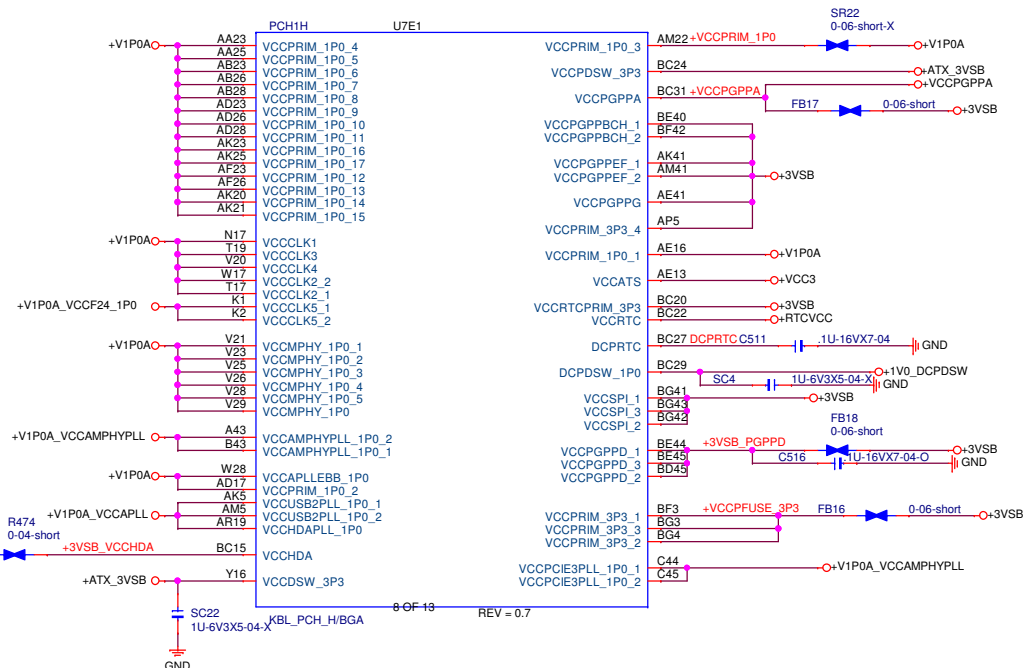
DDC_EN	Passgate
3.3V	Enable
	Disable

HD_HPD	Status
Hi	Plugged
Lo	unplugged

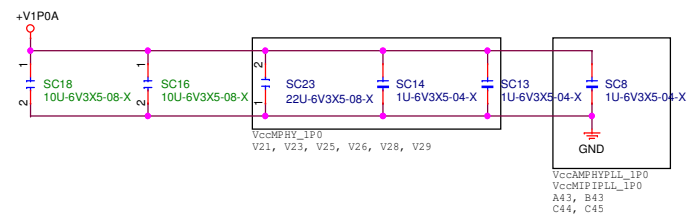
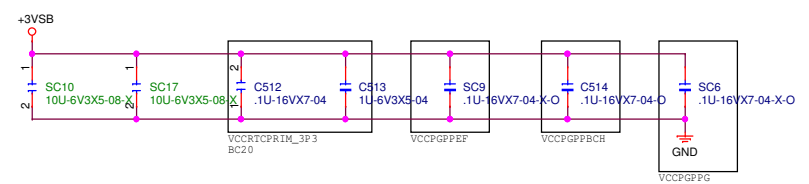
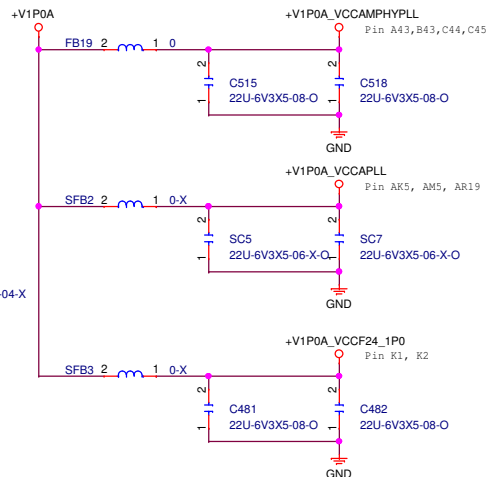
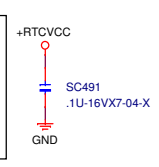
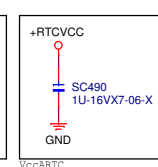
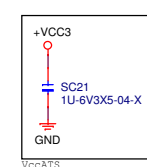
HD_HPD:Internal 100K pull low

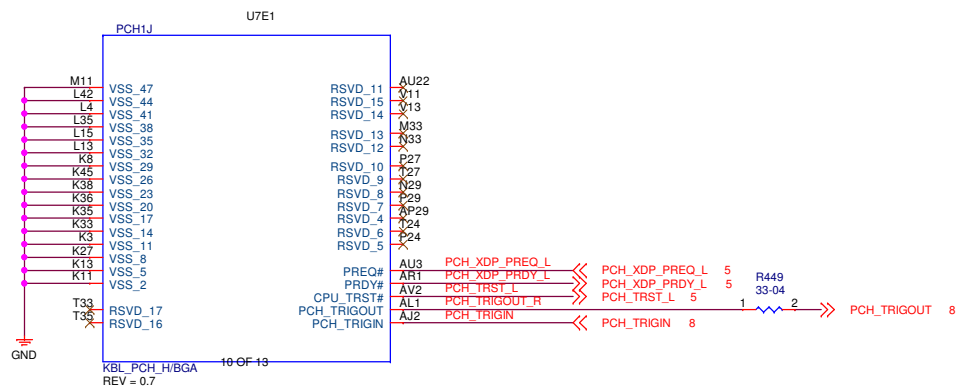




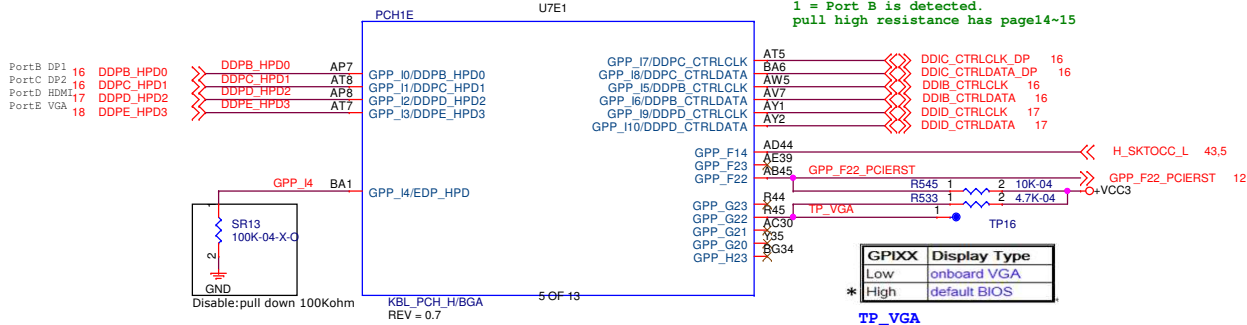


PCH heatsink (T/U phase)
P/N:20-120-013584
HEAT SINK.....SILVER.RHS04441R0.SB.31.5*31*1.5mm....
W/PUSH PIN*2,PAD,FOAM.....LEAD-FREE (RoHS/HF) .ZHIHANG

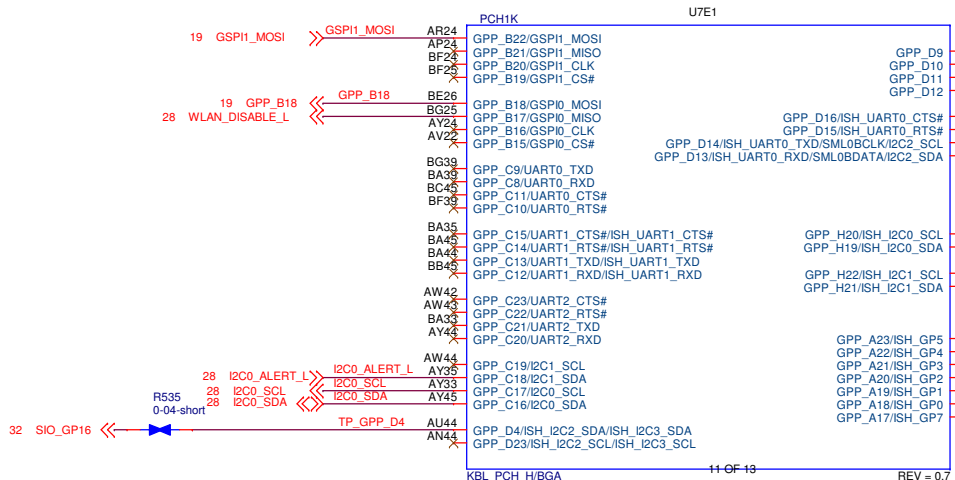
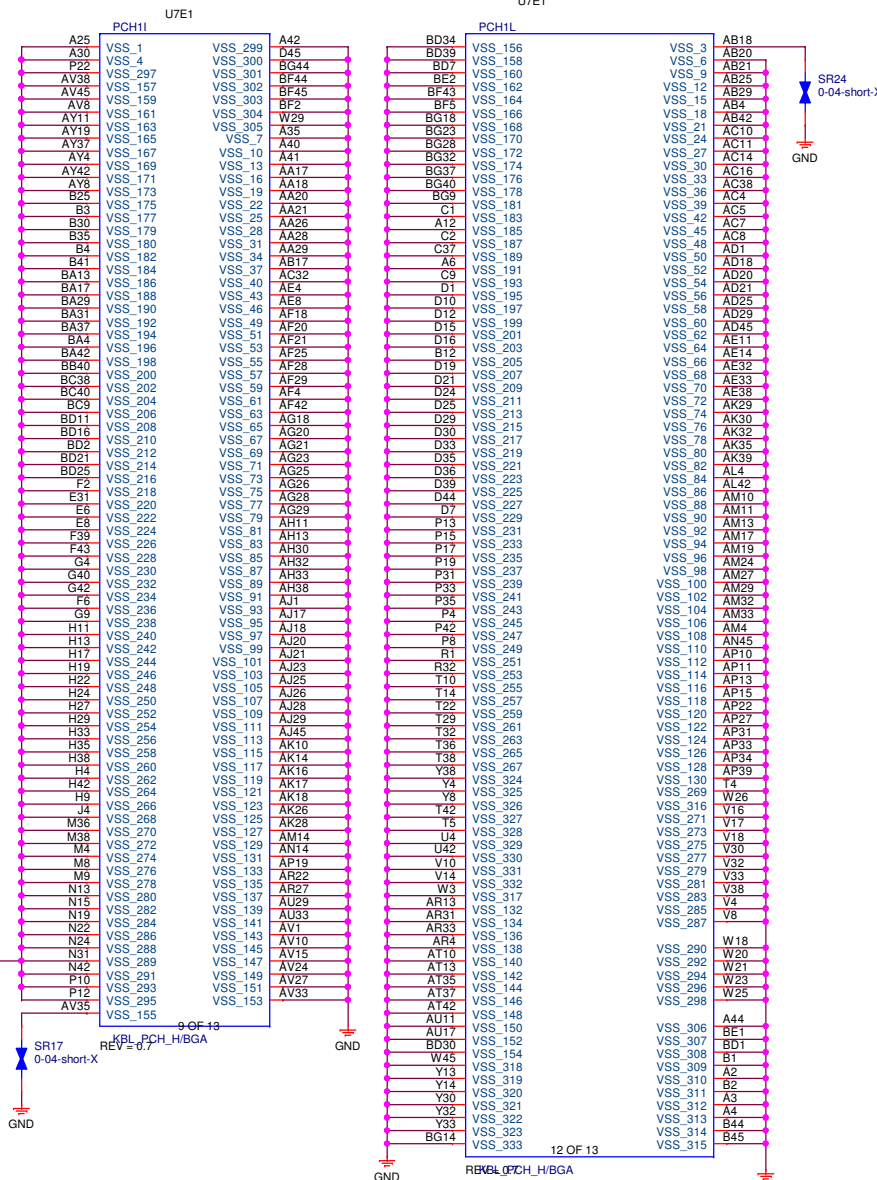


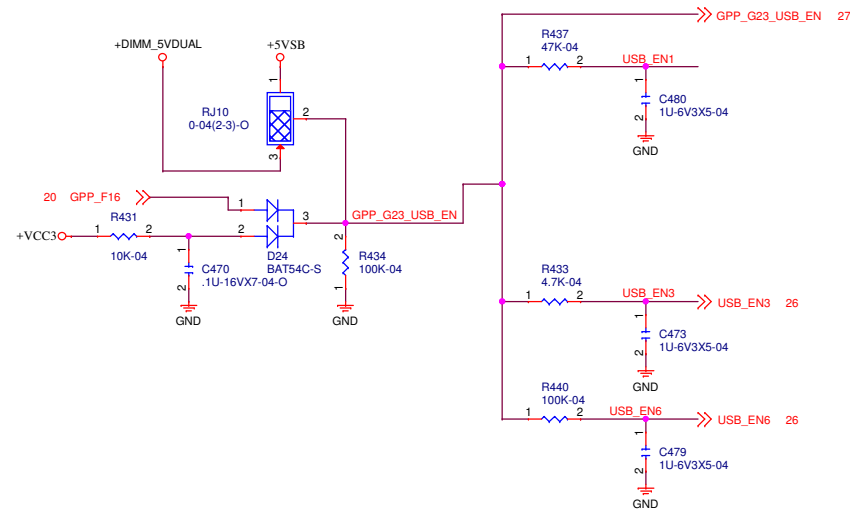


Display Port B/C/D Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.
pull high resistance has page14~15



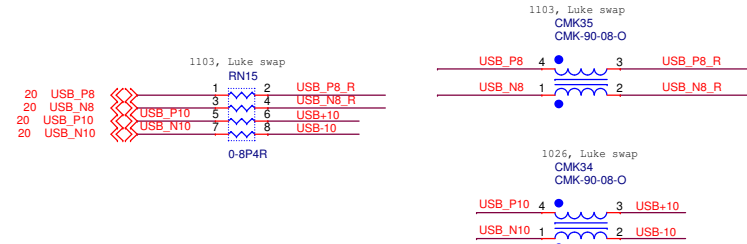
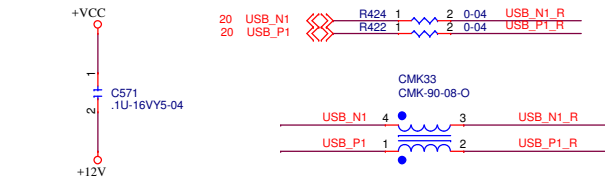
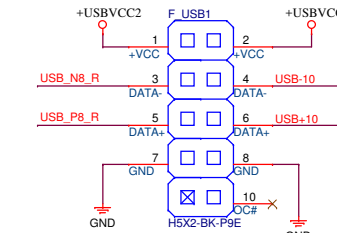
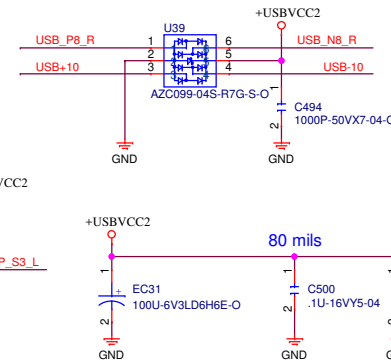
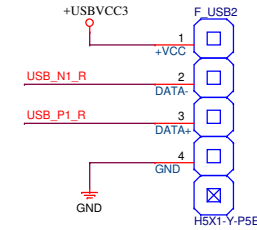
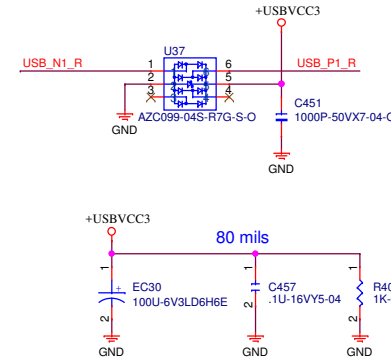
GPIXX	Display Type
Low	onboard VGA
High	default BIOS



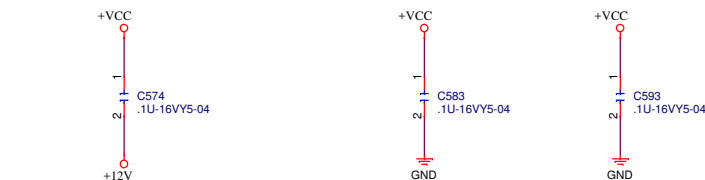


	power switch Enable use	RJ5	D26	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (2-3)	NA	0 Volt	Acer S4 W S5 W/O USB_5VDUAL
	5VSB	0ohm (1-2)	NA	5 Volt	
*	GPIO	NA	Stuff	S4 : 5 Volt S5 : 0 Volt	

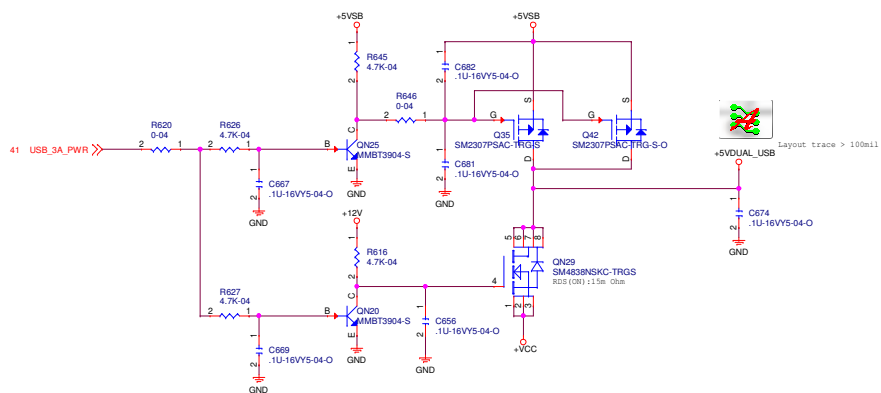
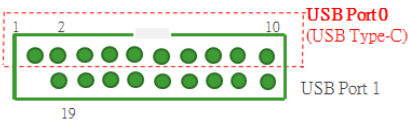
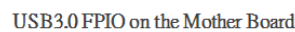
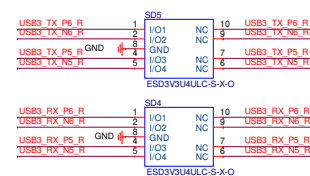
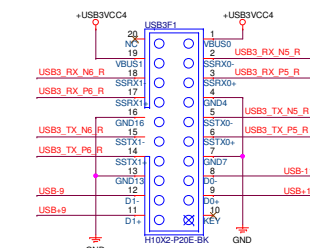
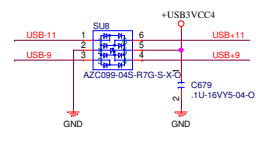
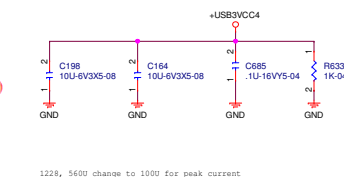
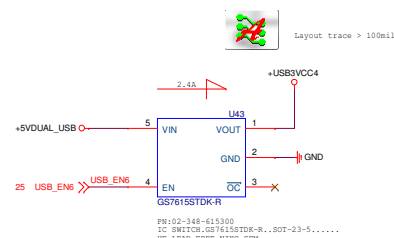
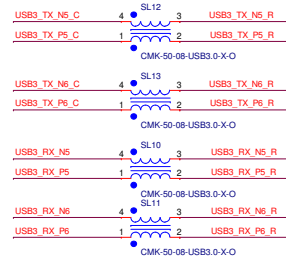
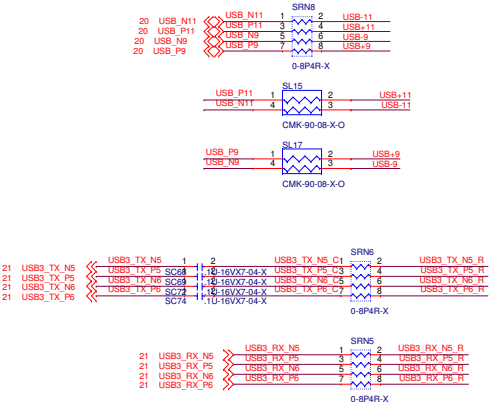
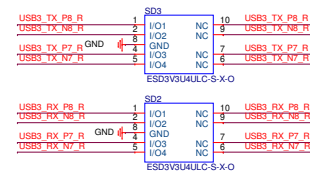
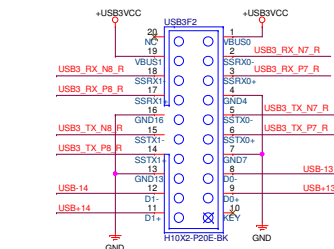
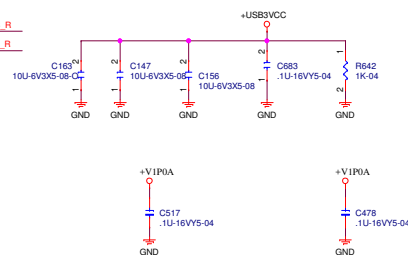
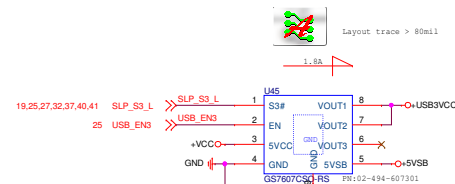
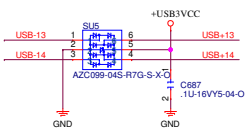
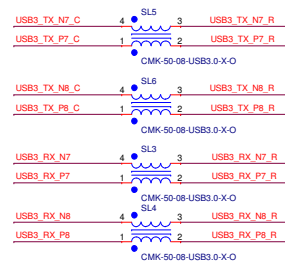
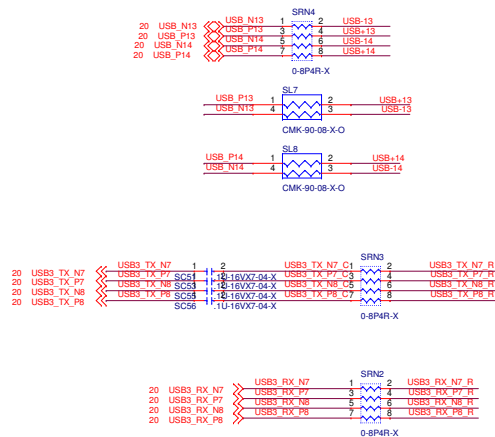
STATUS	S0	S3	S4	S5
GPP_F16	HI	HI	HI	LOW
USB_PWR	ON	ON	ON	OFF




19,26,27,32,37,40,41 SLP_S3_L SLP_S3_L

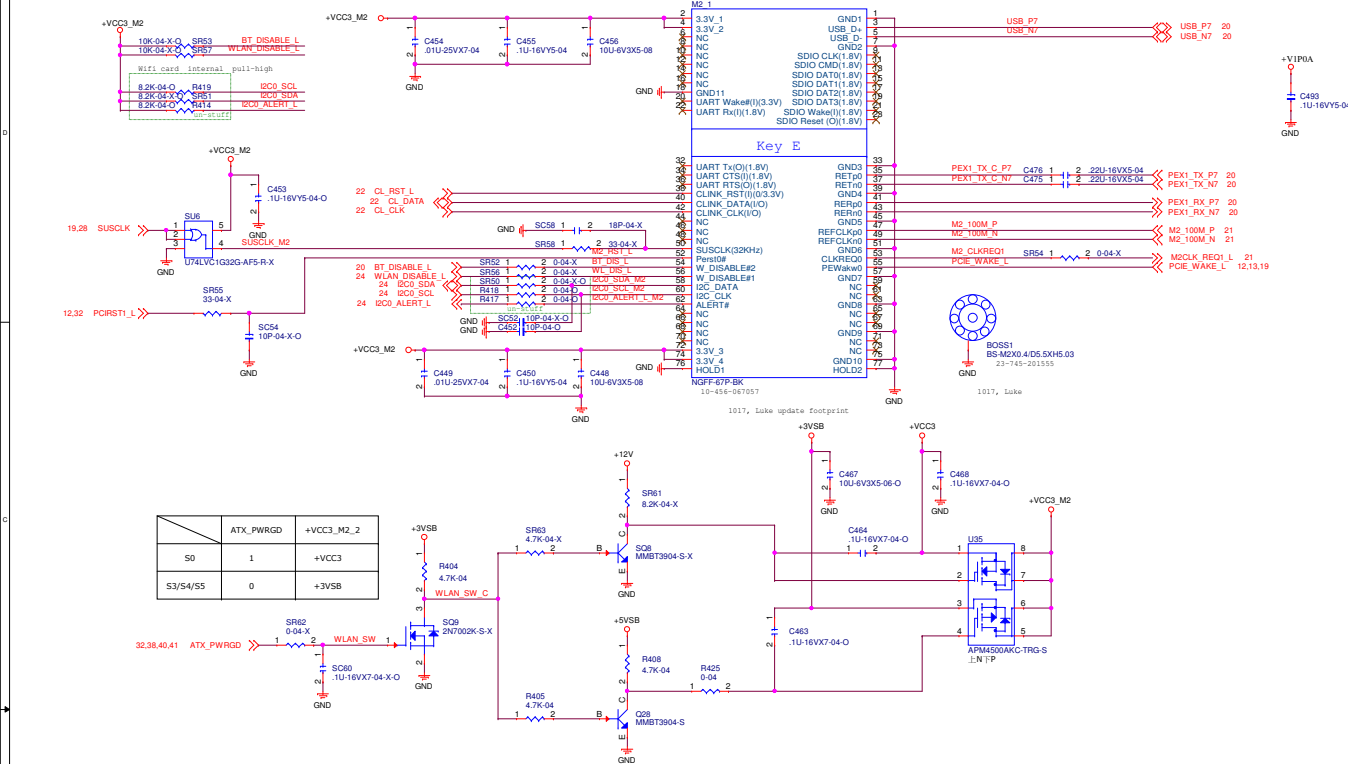


For Q270 only

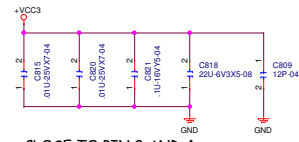
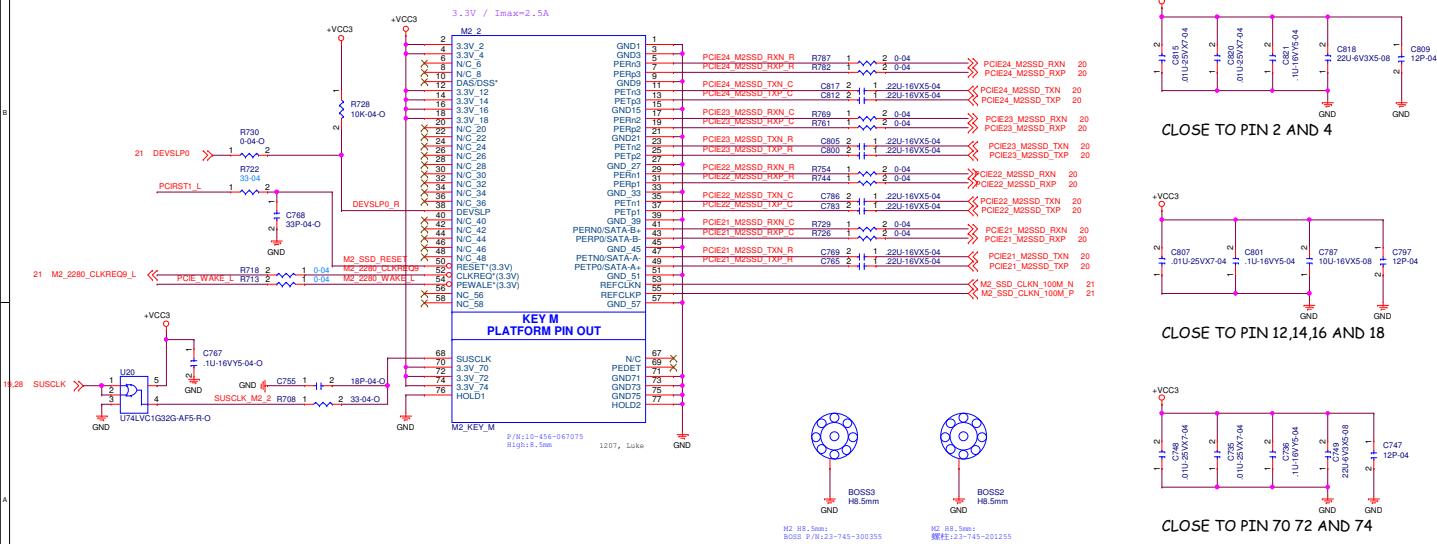


 Elitegroup Computer Systems			
Title USB3.0 Header*2			
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Custom	Q27H4-AM		1
Date:	Thursday, March 30, 2017	Sheet	26 of 49

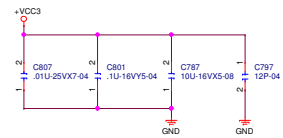
M.2 WIFI



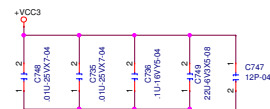
M.2 SSD



CLOSE TO PIN 2 AND 4

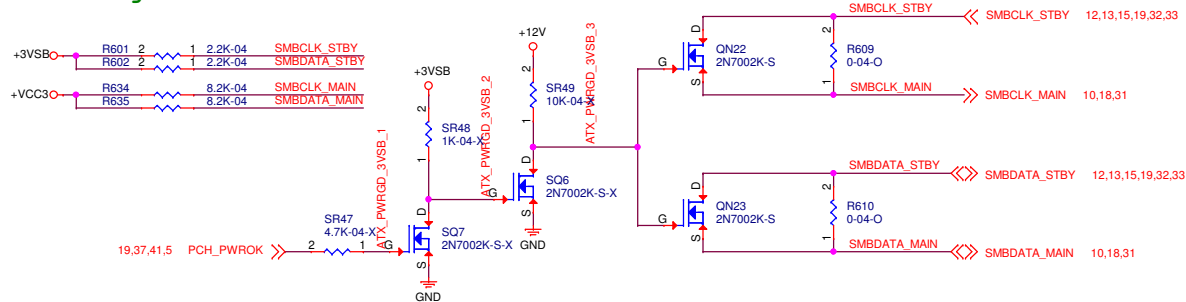


CLOSE TO PIN 12,14,16 AND 18

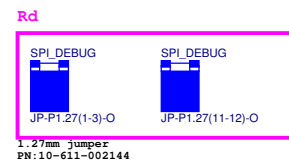
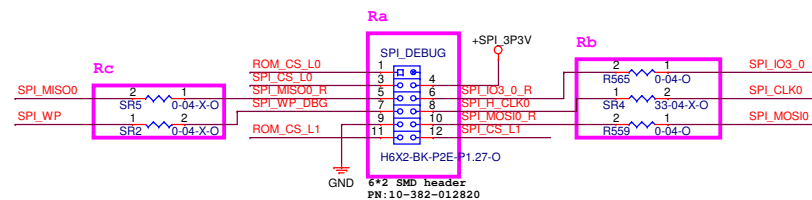
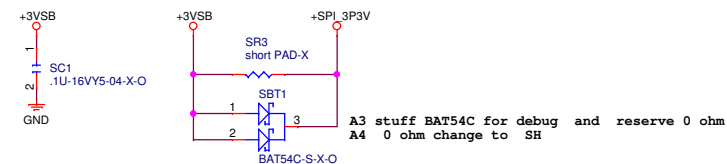
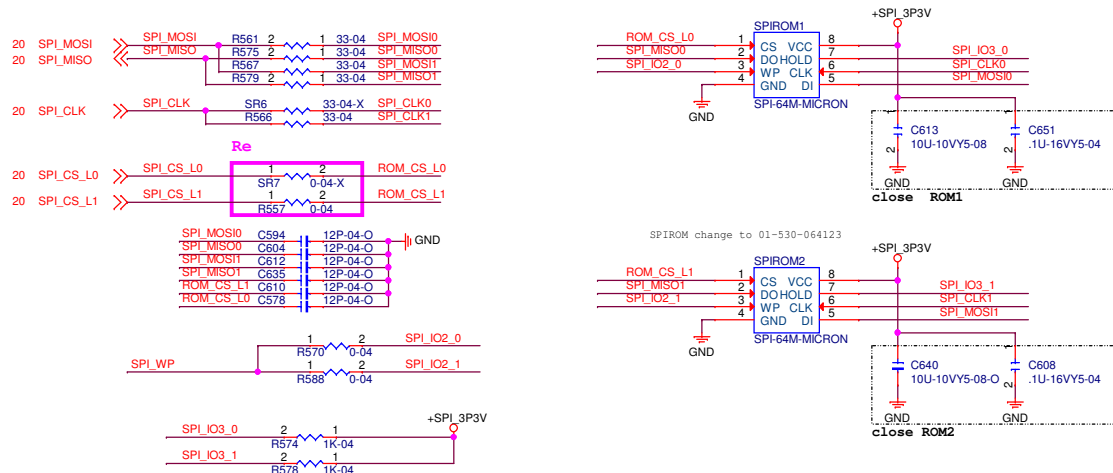


CLOSE TO PIN 70 72 AND 74

SMbus Logic Circuit

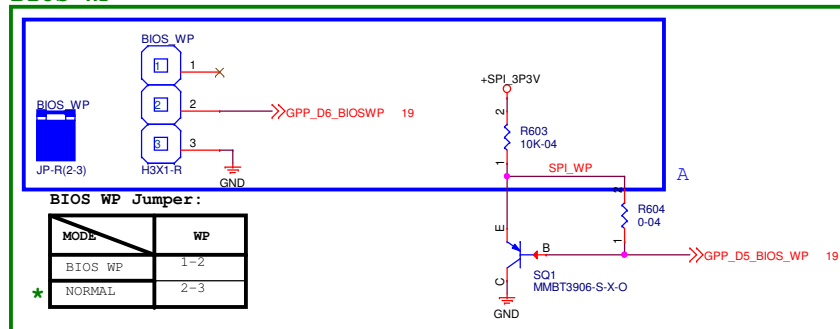


SPI ROM

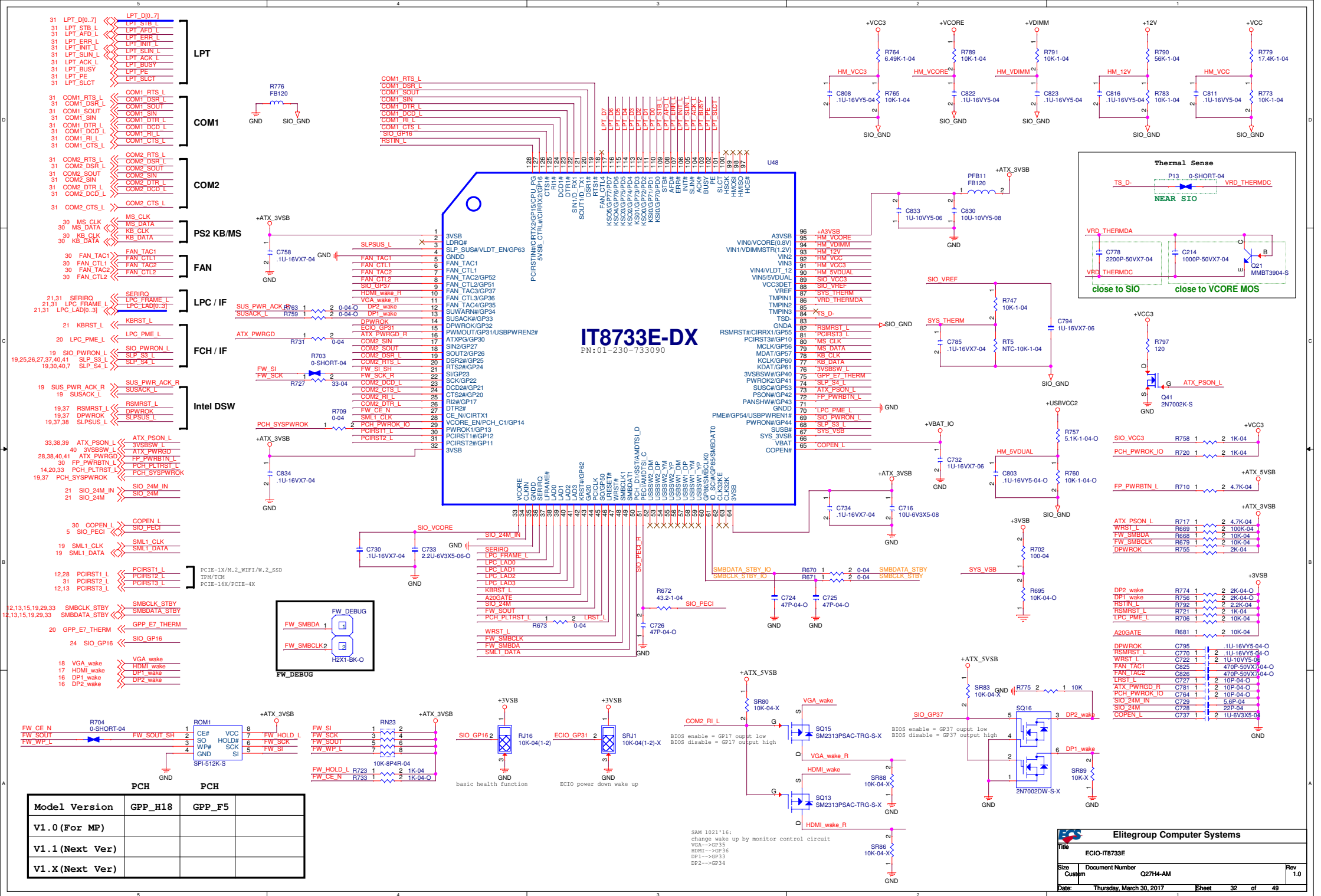


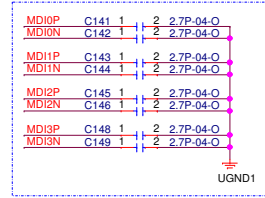
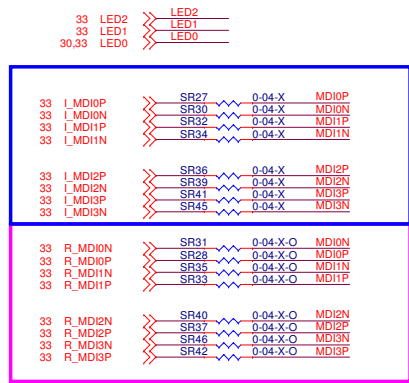
	Ra	Rb	Rc	Rd	Re
A3~A5	O	O	O	O	X
MP	X	X	X	X	O

BIOS WP

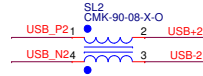
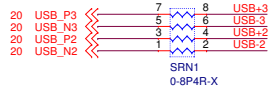
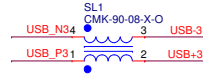




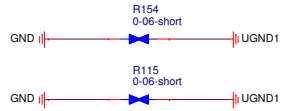




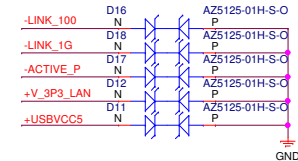
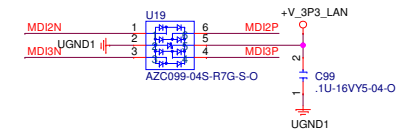
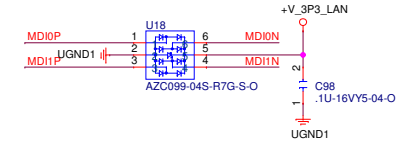
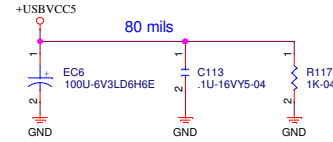
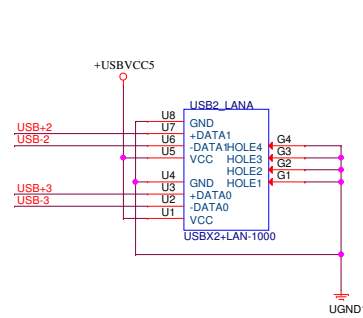
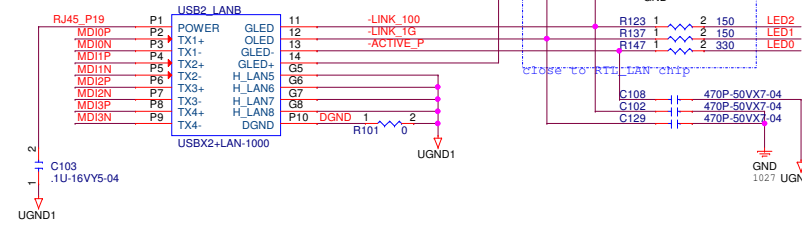
For EMI



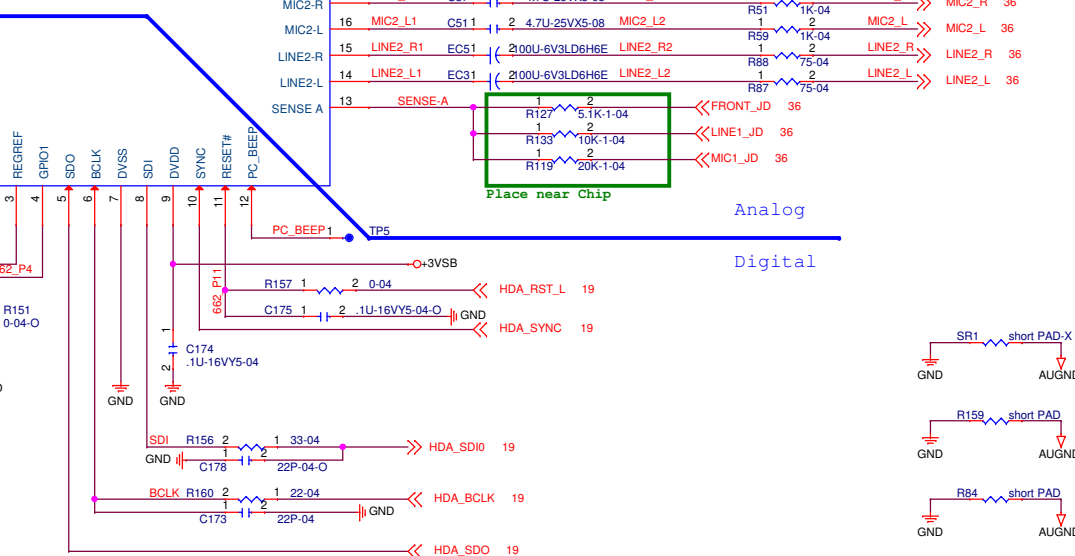
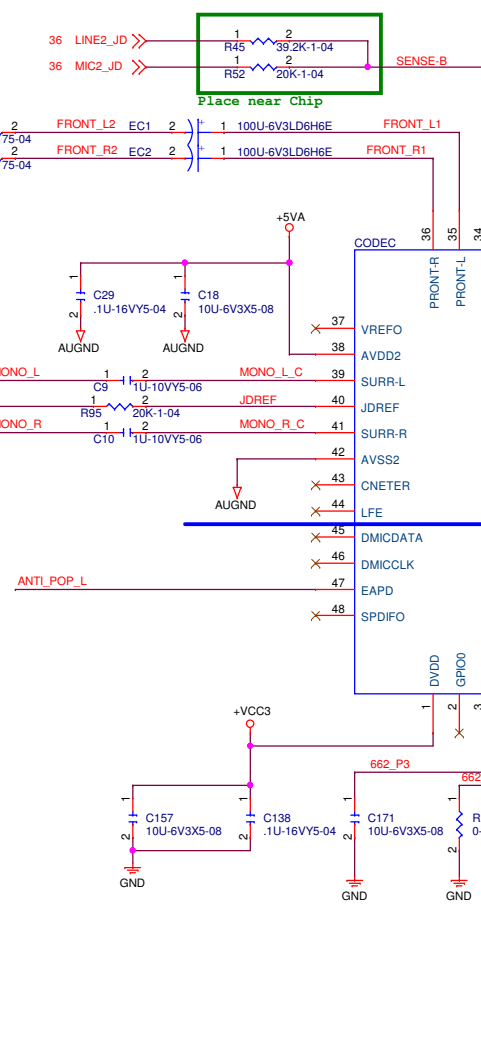
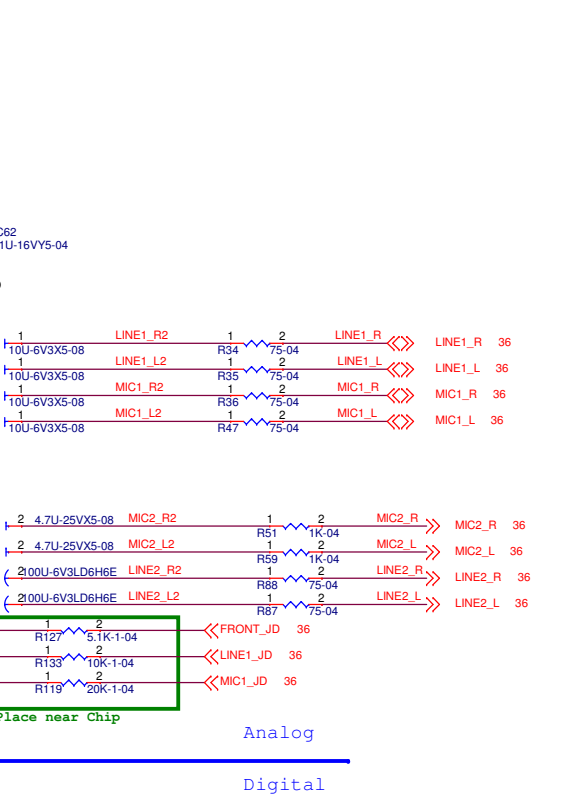
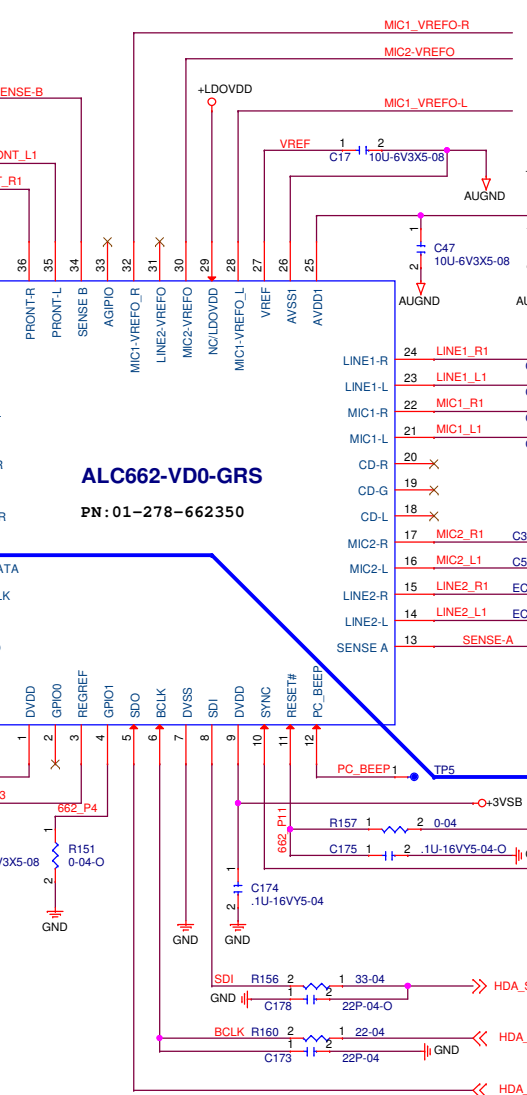
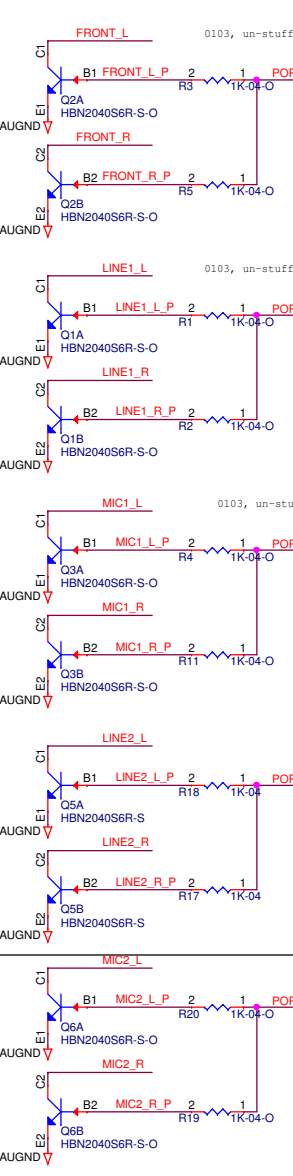
Close to LAN connector

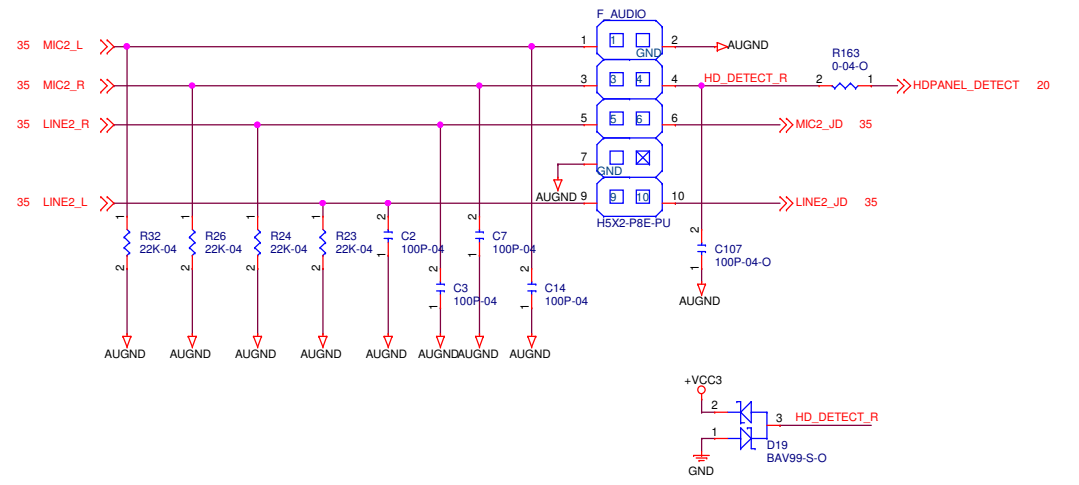
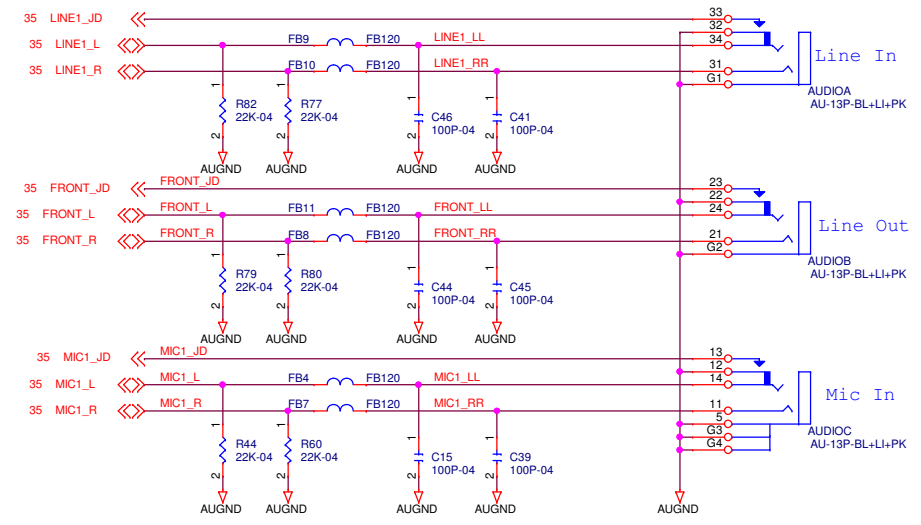
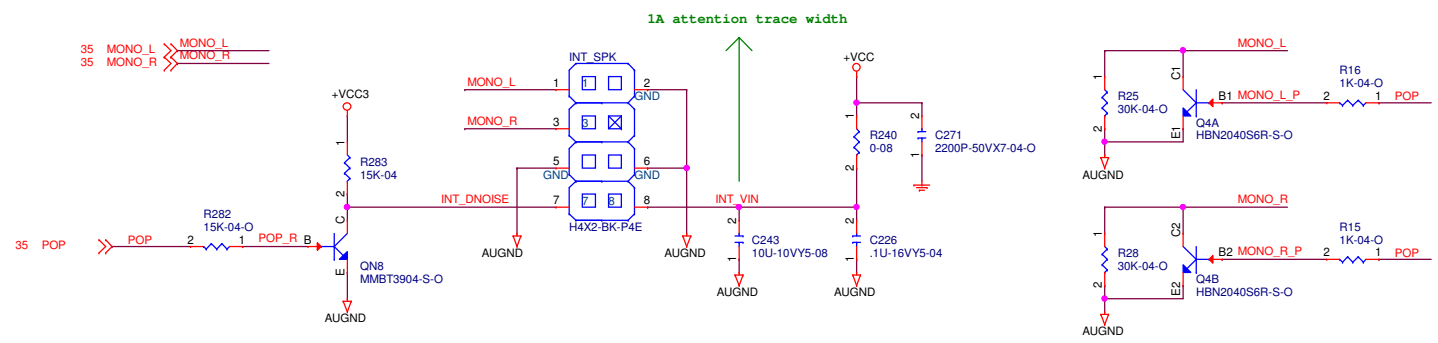


USB2.0+LAN

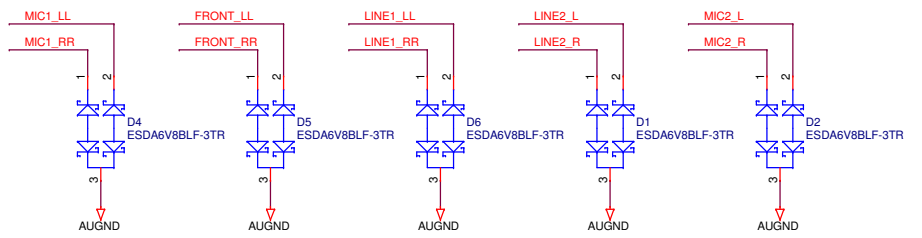


				S0	S3	S4	S5	G3 to S5
<div>Rear Side</div> <div>ActiveSpeed</div>	Active LED (Single Color)	Access	Blink		Blink	Blink	Blink	
		Not Access	OFF		OFF	OFF	OFF	
	Speed-LED (Dual Color)	Disconnected	OFF	OFF	OFF	OFF		
		1000: ON with Amber Color	ON					
		100: ON with Green Color	ON					
		10: OFF	OFF					



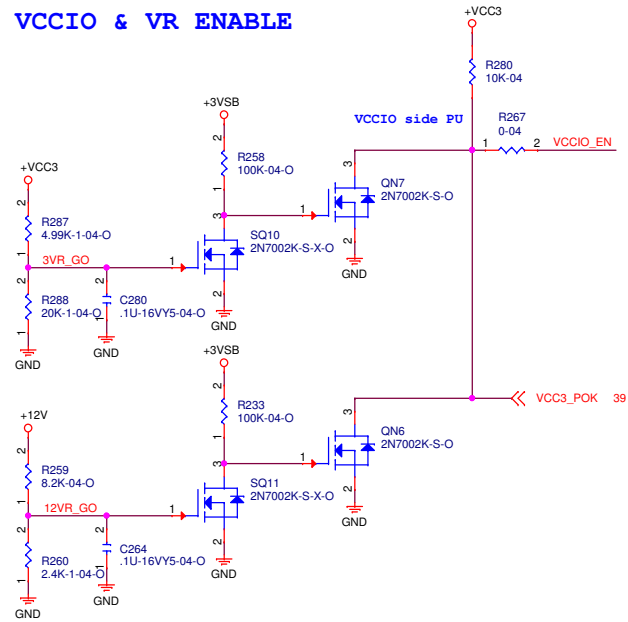


A	B	C
	PIN	FUNCTION
LINE IN	3Q	LINE IN-JD
	3P	AUGND
	31	LINE IN_L
	34	LINE IN_R
LINE OUT	G1	AUGND
	2Q	LINE OUT-JD
	2P	AUGND
	21	LINE OUT_L
MIC IN	24	LINE OUT_R
	G2	AUGND
	1Q	MIC IN-JD
	1P	AUGND
MIC IN	11	MIC IN_L
	14	MIC IN_R
	5	AUGND

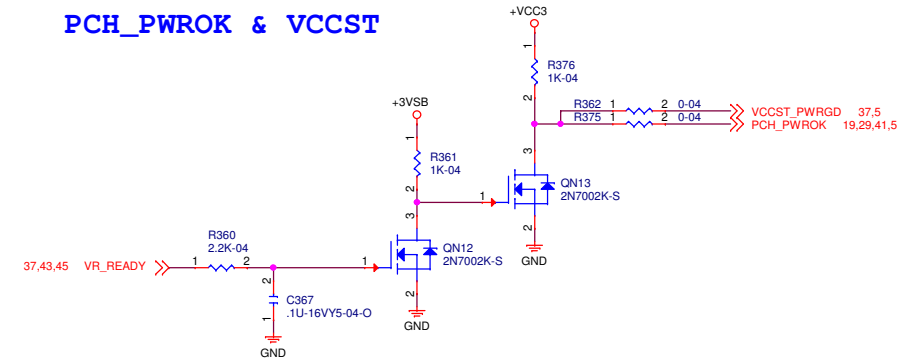


PN:03-100-700872
TVS ARRAY..ESDA6V8BLF-3/TR..SOT-23.5V.....LEAD-FREE (RoHS/HF) .WILLSEMI

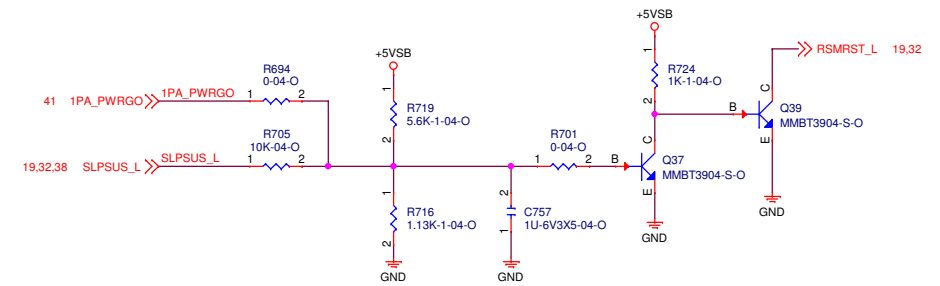
VCCIO & VR ENABLE



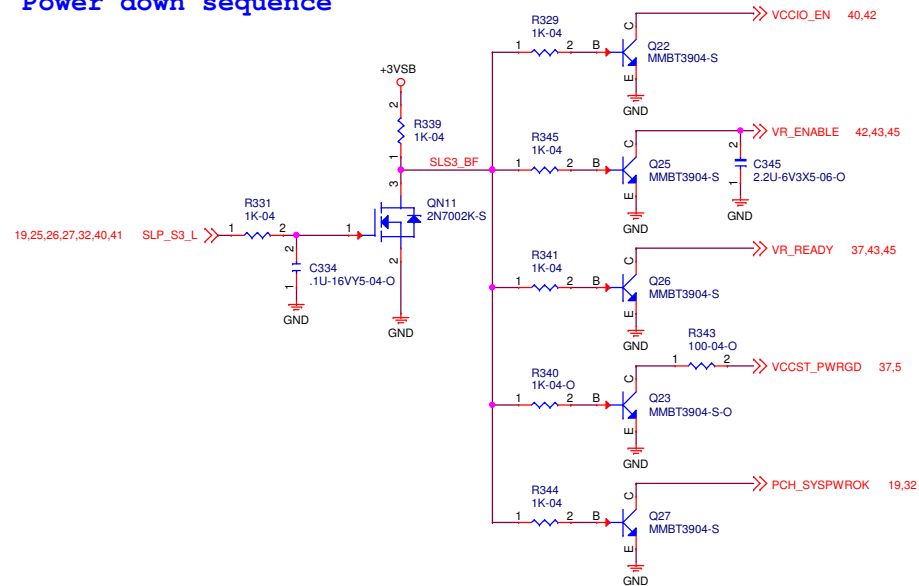
PCH_PWROK & VCCST



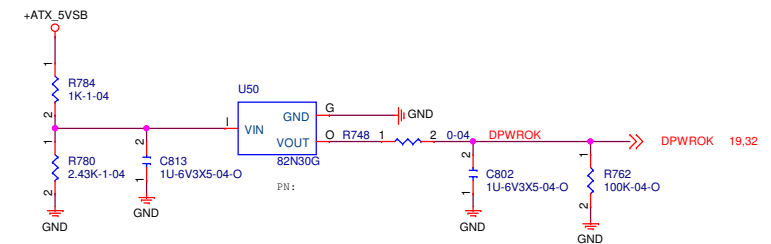
RSMRST#

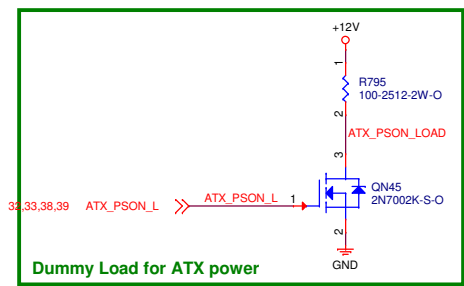
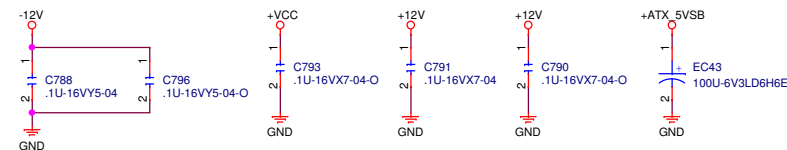
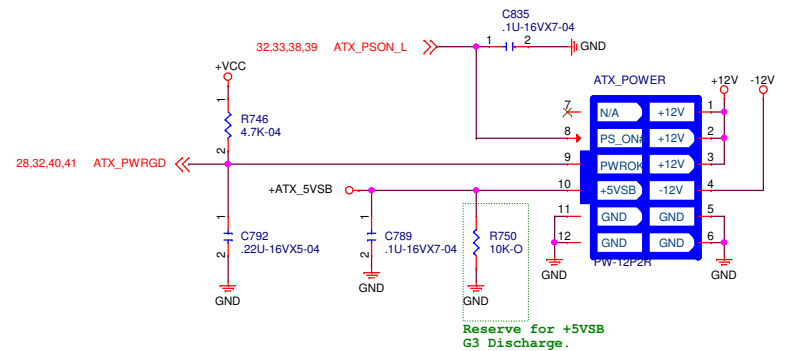


Power down sequence

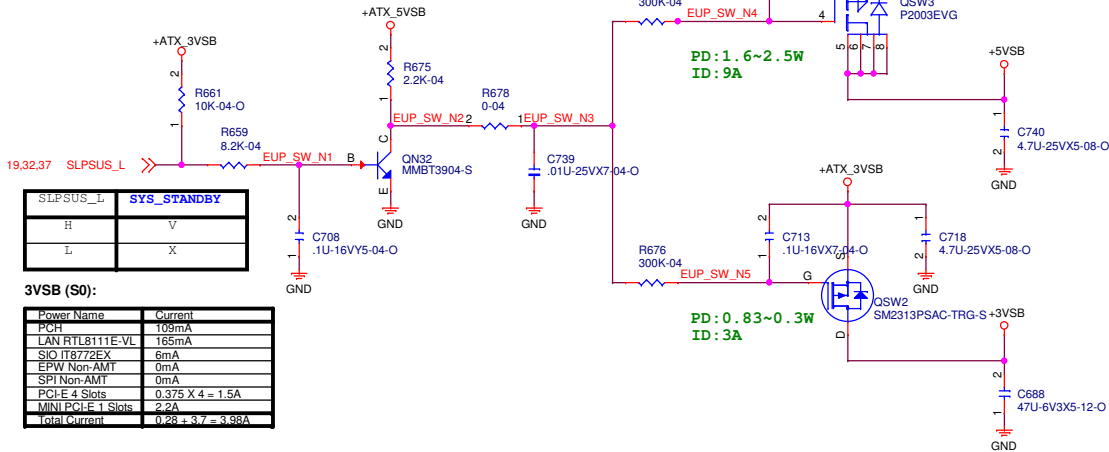


DPWROK



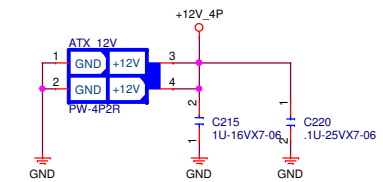


EuP Lot6 Power Saving Circuit



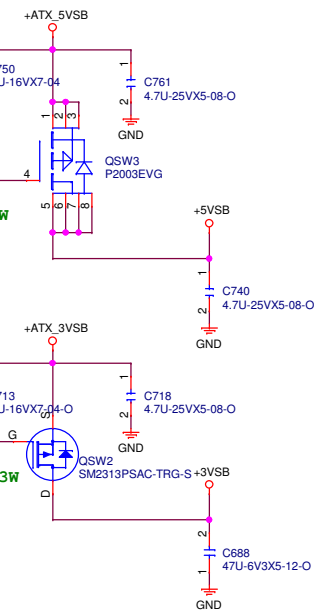
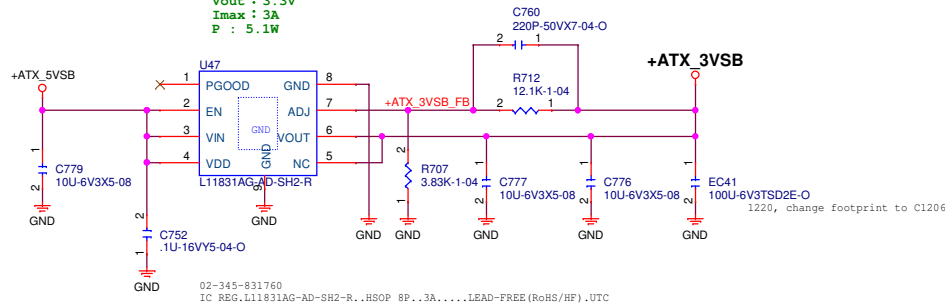
SLPSUS_L	SYS_STANDBY
H	V
L	X

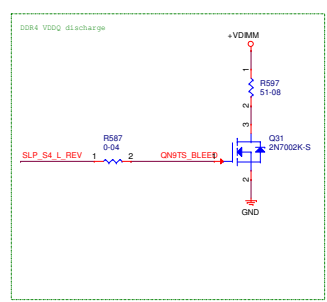
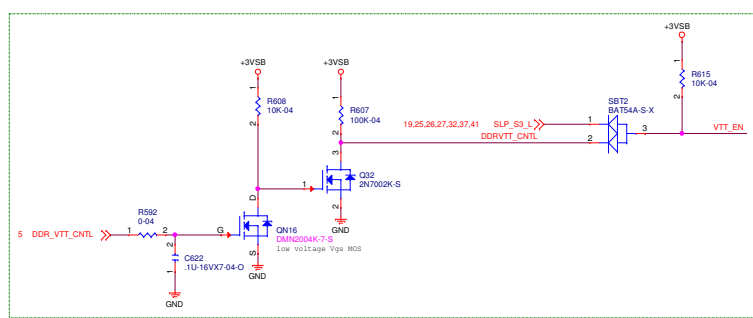
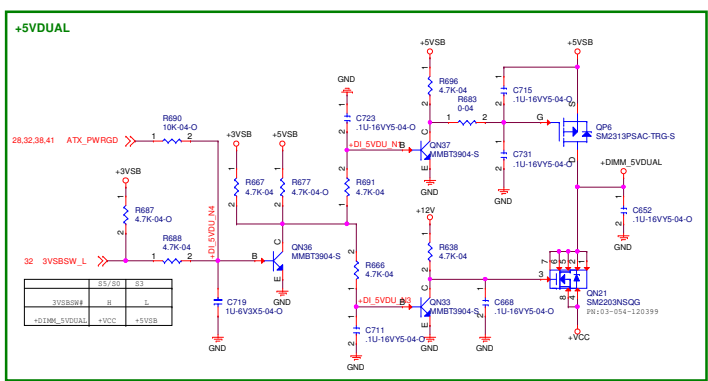
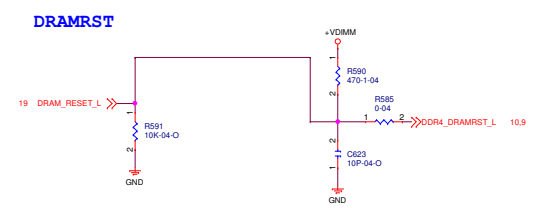
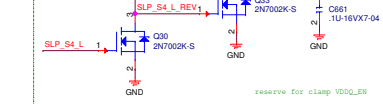
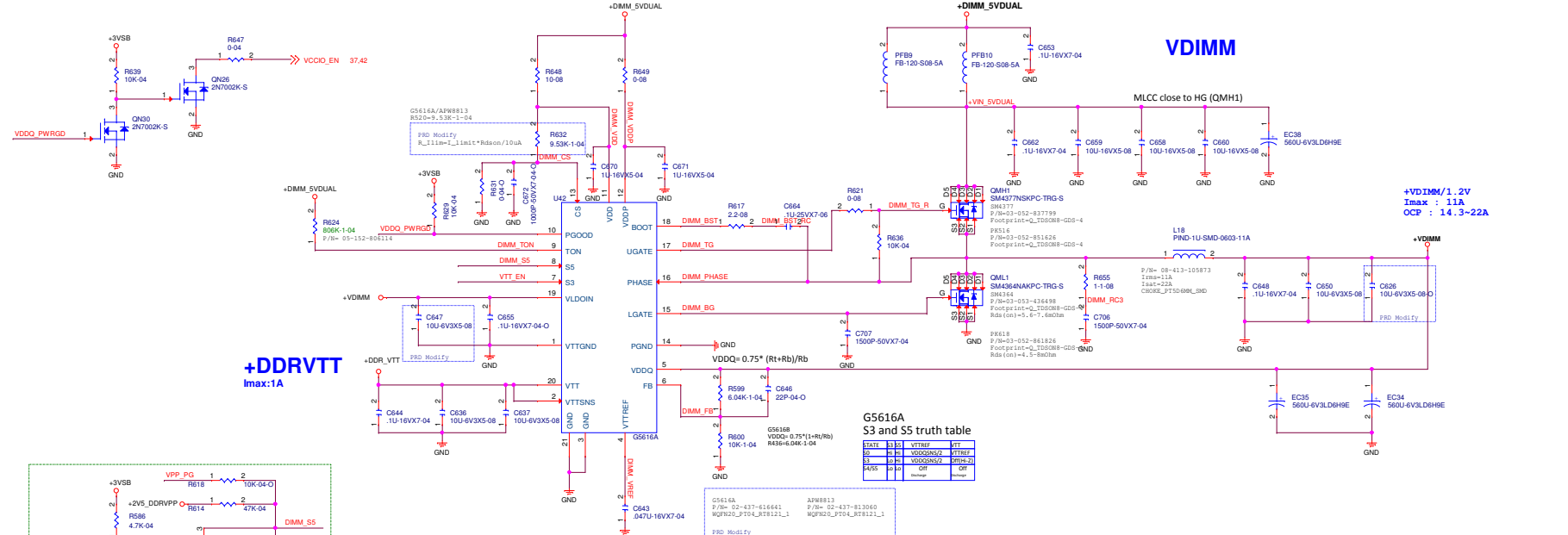
Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO I6772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	2.2A
Total Current	0.28 + 3.7 = 3.98A

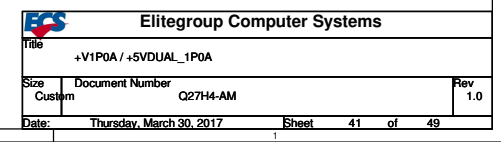


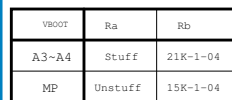
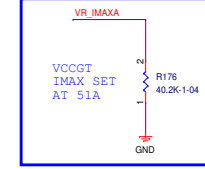
+ATX_3VSB

Vout : 3.3V
Imax : 3A
P : 5.1W





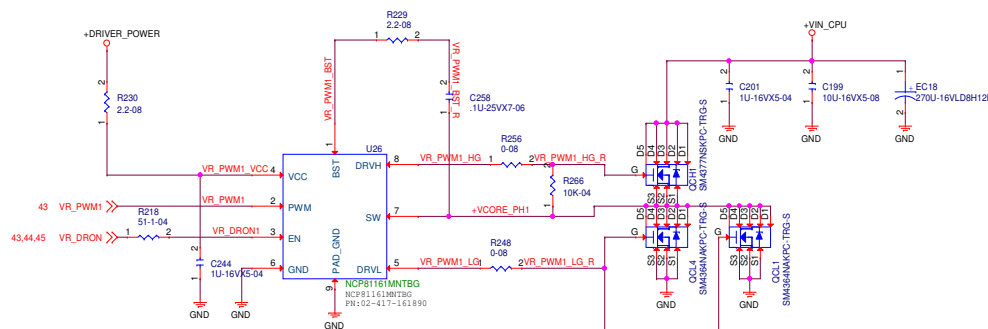
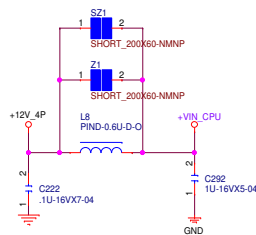
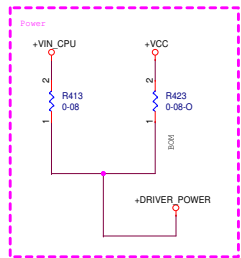




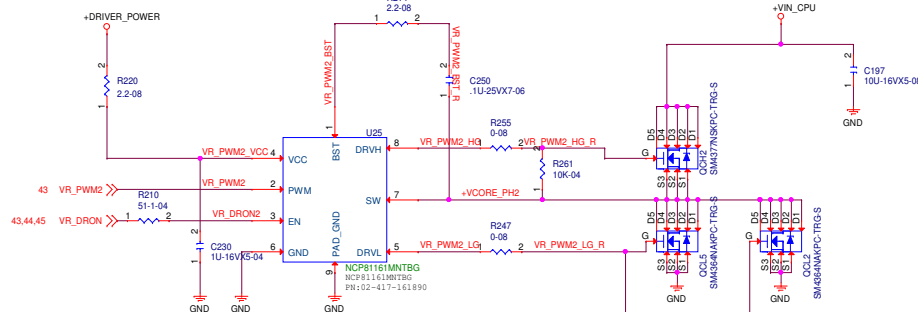
SKL-S VCCVID 0.55~1.5V
42 65W 35W
TDC 61A 53A
IMAX 79A 66A

Imax : 79A
94.8~118.5A (Vendor Check)

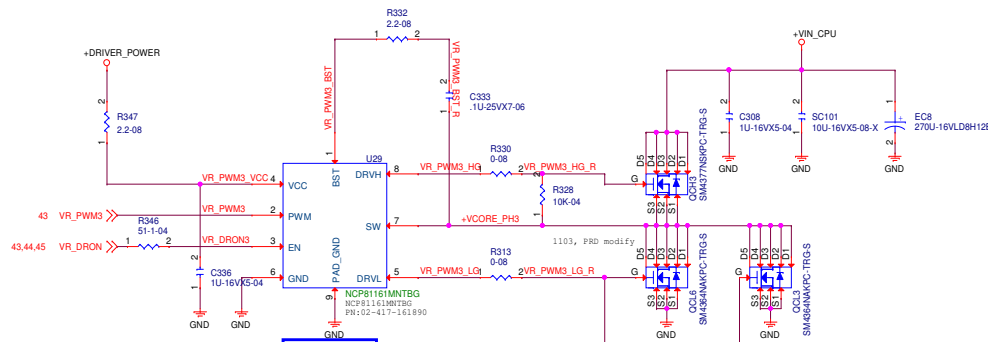
Vin = 12V
Fs = 340khz
Iout = 79A
Vin Irms = 8.23A
MLCC ripple current = 3A
LIR = 37.2%
Cin_cap = 270uF*3, 4.7uF*3
Cout_cap = 560uF*5
OCP = 94.8~118.5A



BOTTOM PAD
CONNECT TO
GND Through
4 VIAs



BOTTOM PAD
CONNECT TO
GND Through
4 VIAs



BOTTOM PAD
CONNECT TO
GND Through
4 VIAs

